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# MS-7975

## Intel -Skylake plamform B150

mATX

Ver: 0A ( 243.84 x 190 )

**CPU:**  
SKL-S LGA1151

**System Chipset:**  
SPT-H B150

**Onboard Chipset:**  
SIO: Nuvoton 6793D  
Flash ROM: SPI 128Mb  
HD Audio Codec: ALC892  
LAN: RTL8111EPV coly RTL8111G

**PWM:**  
VCORE - RT3606  
DDR - RT8125  
PCH - RT8125  
VCCSA - RT8125  
VCCIO - (Converter)

**LDO:**

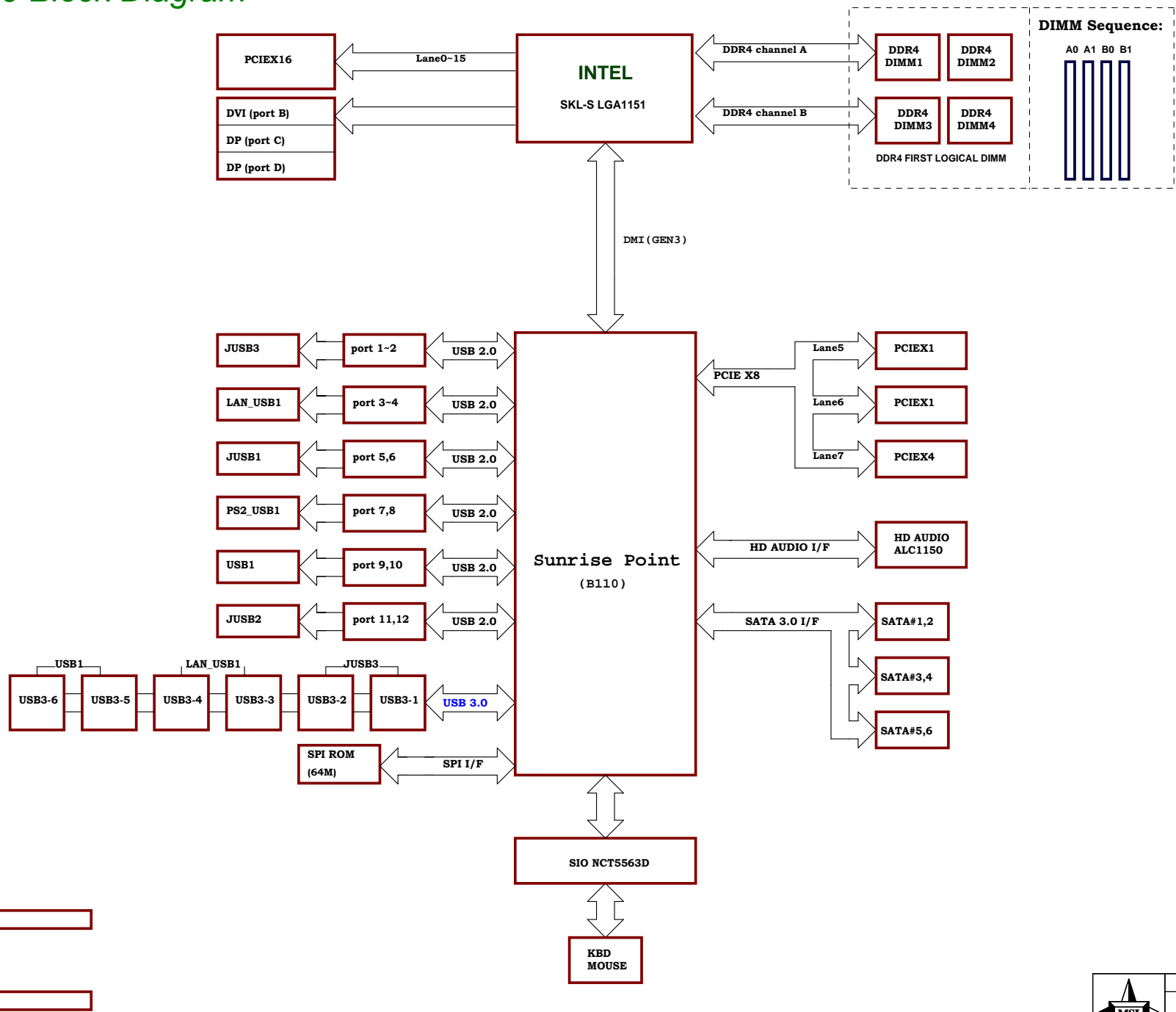
**Main Memory:**  
DDR4 \* 4

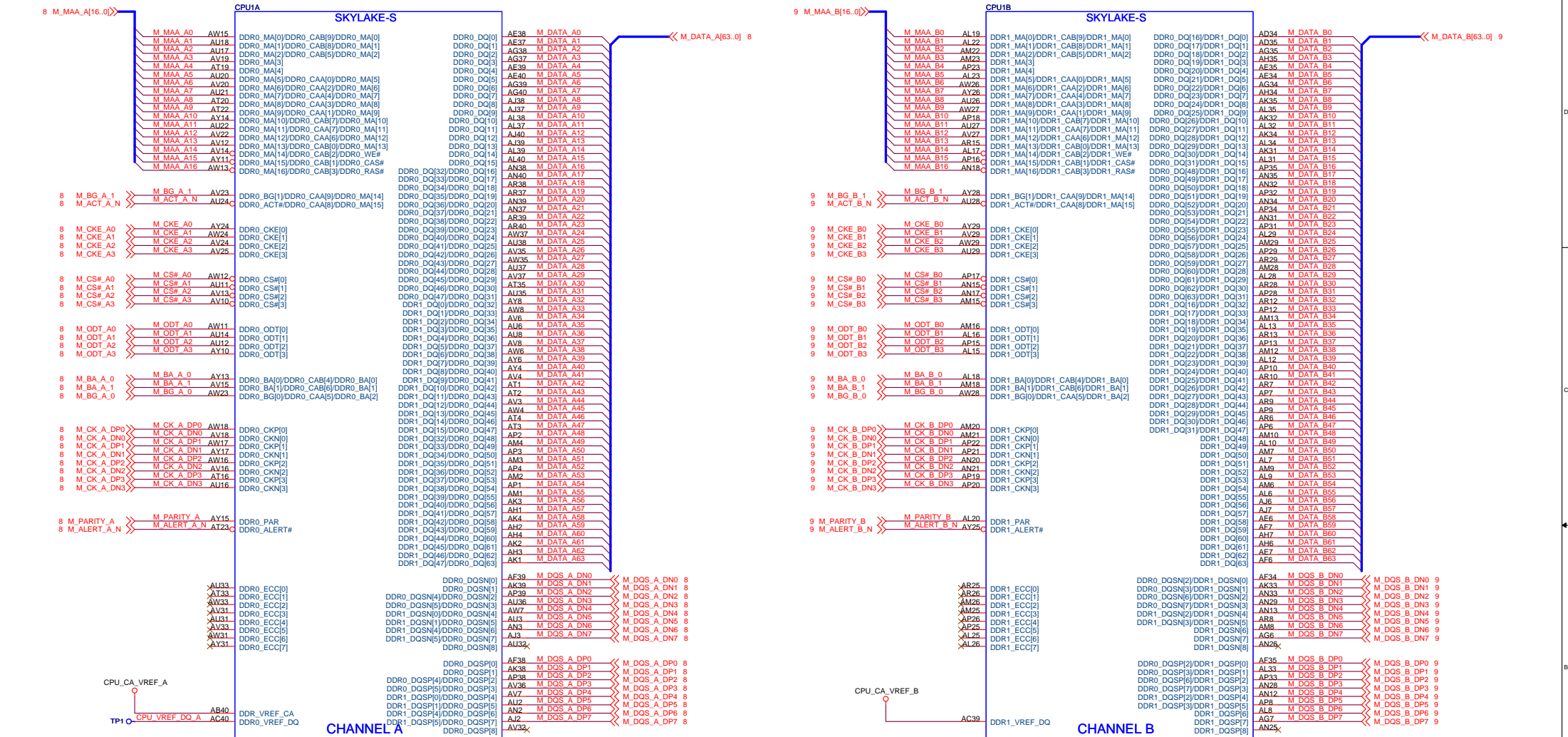
**Expansion Slots:**  
PCI Express (X16) Slot \* 1  
PCI Express (X1 ) Slot \* 1  
PCI Express (X4 ) Slot \* 1  
PCI Slot \* 1

**Other:**  
SATA3.0 \* 6  
FRONT USB2.0 \* 2  
FRONT USB3.0 \* 4  
REAL USB2.0 \* 2  
REAL USB3.0 \* 4

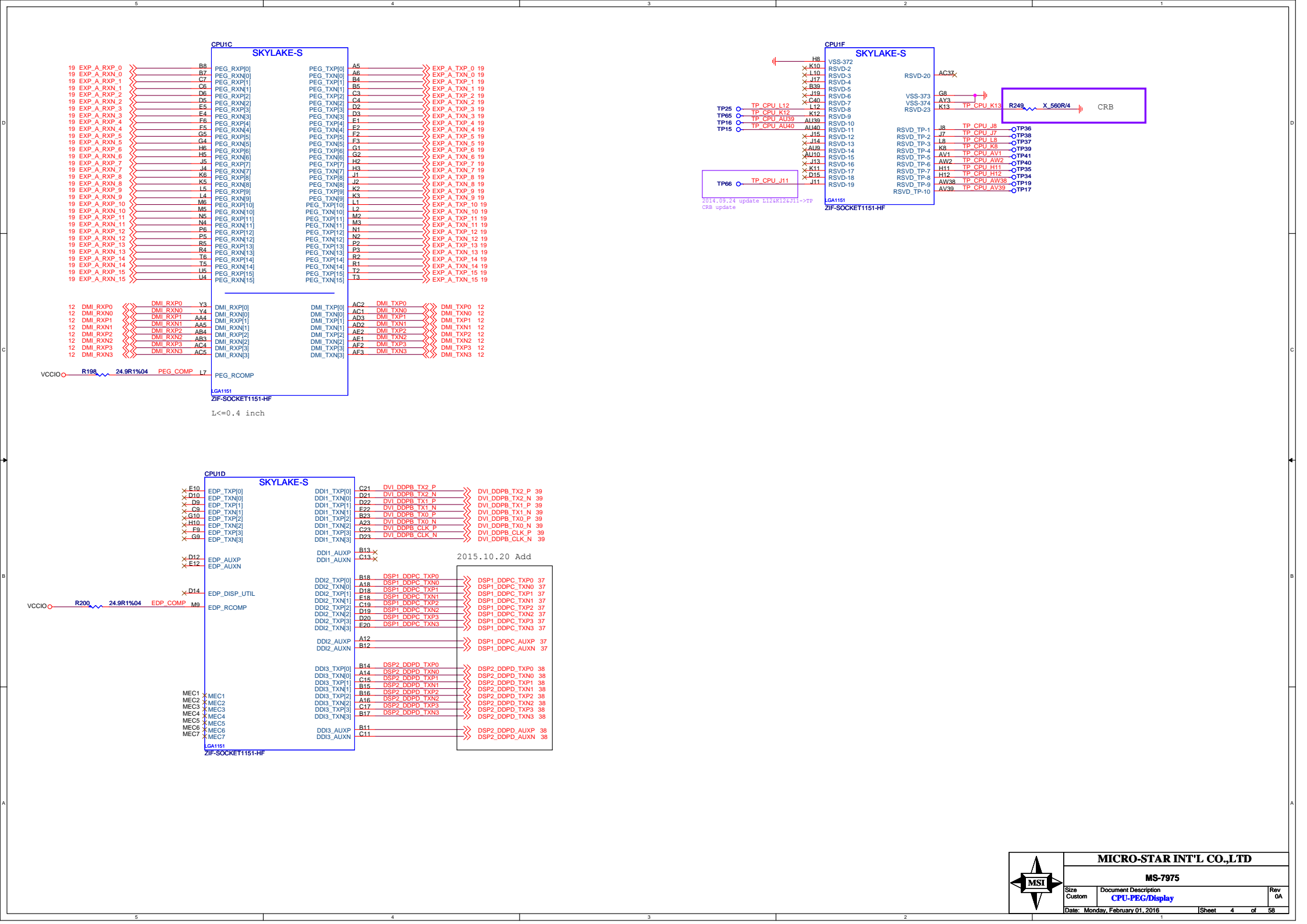
**ACPI:**  
5VDAUL:uP7501  
5VDIMM:uP7501  
3VSB:GS7166+N MOS  
3VDSW:GS7166

# MS-7979 Block Diagram

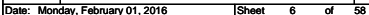


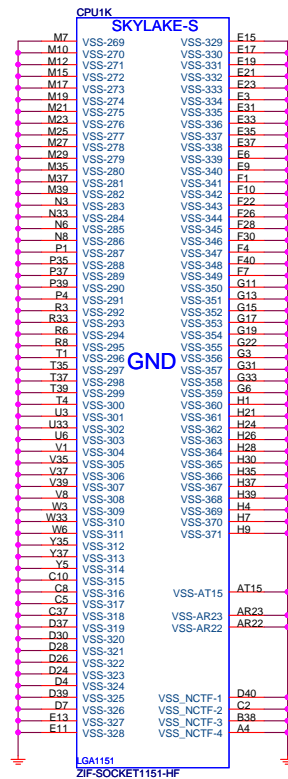
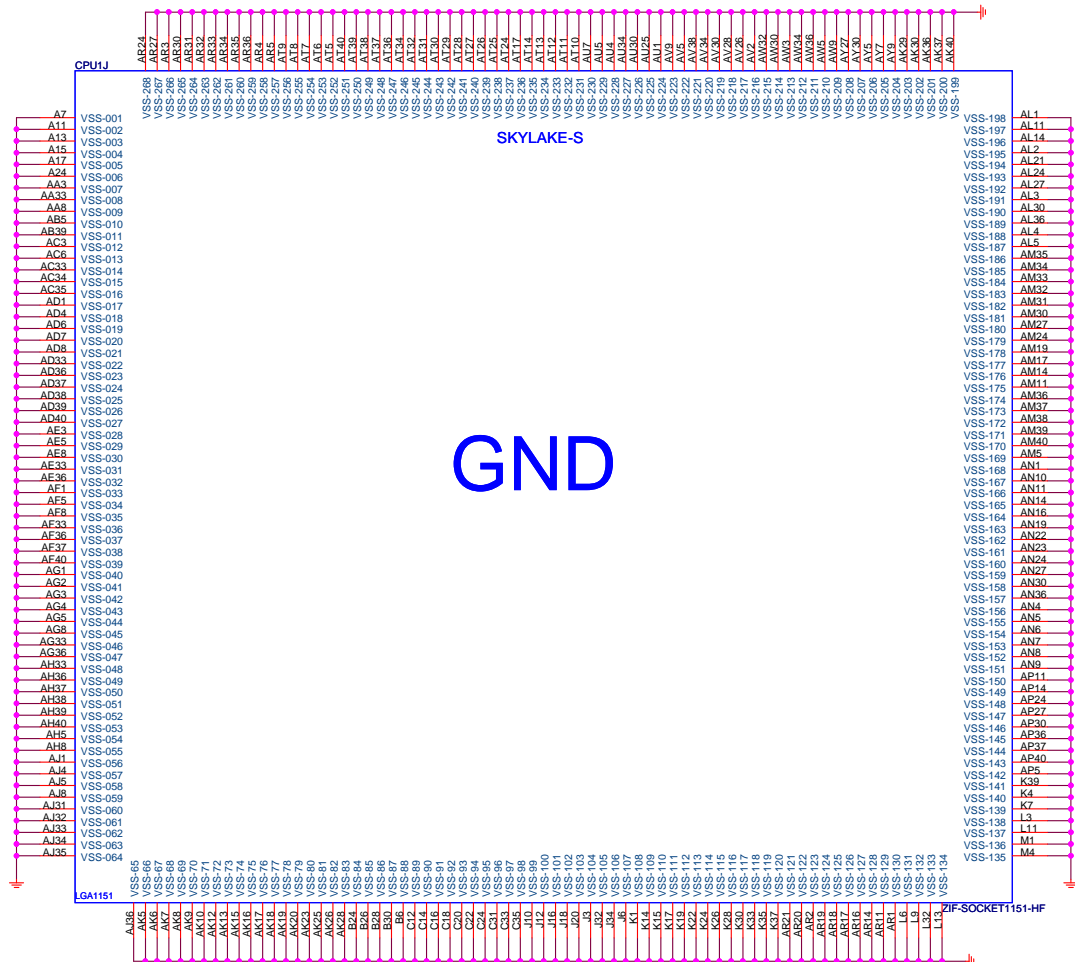


DDR3: CPU\_DQ\_VREF\_A  
DDR4: NA  
See Page11 circuit

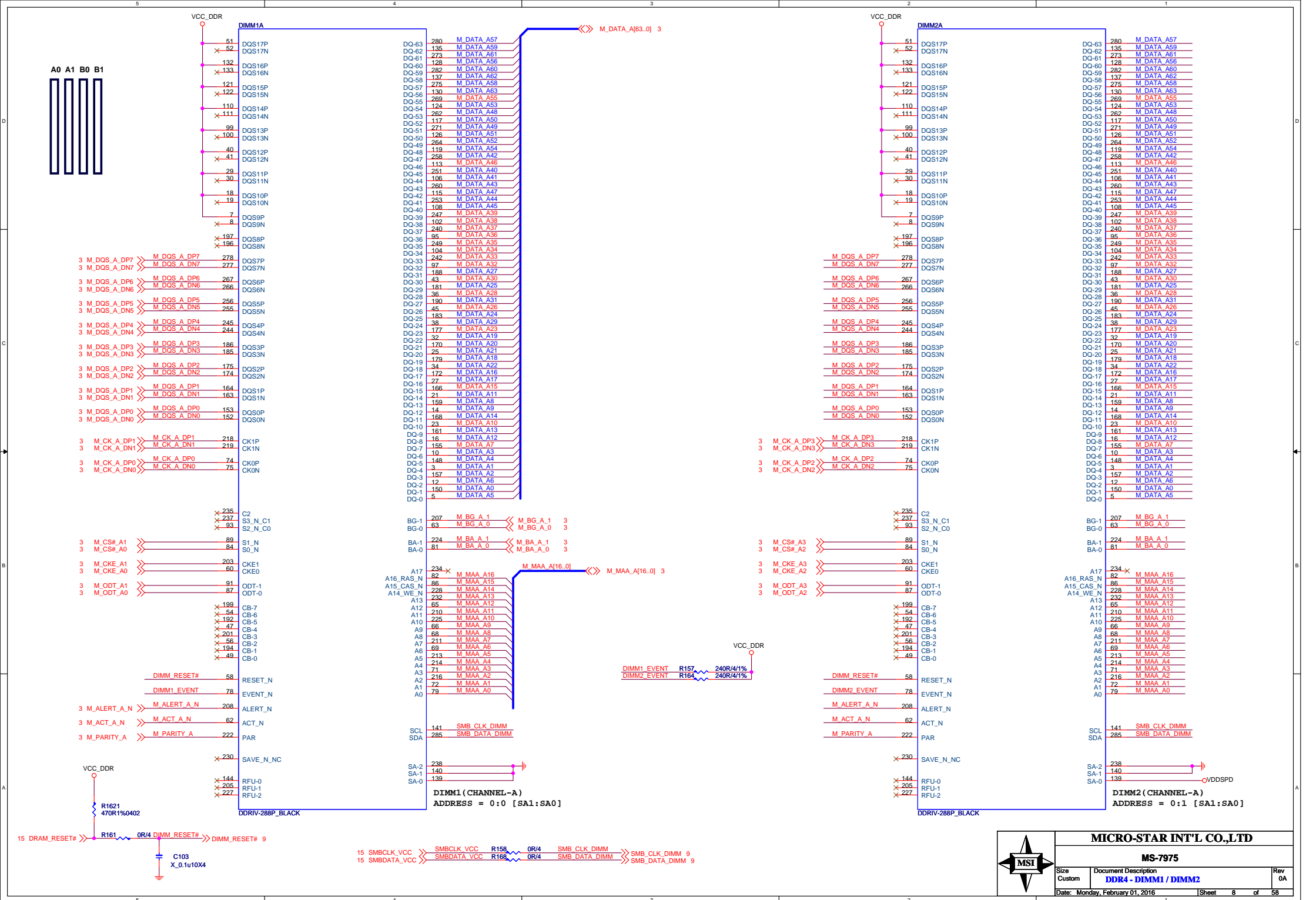






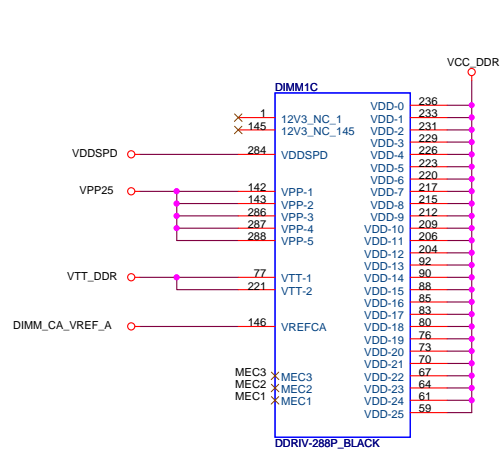




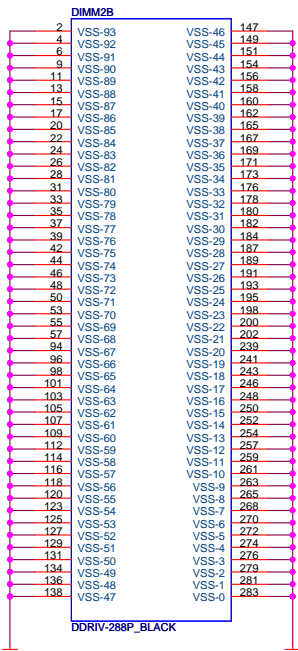
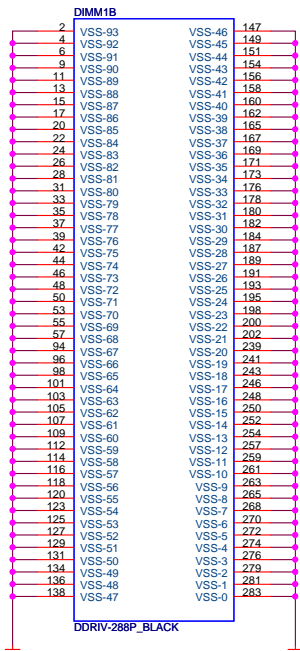
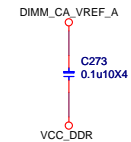
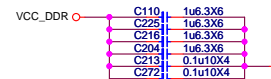
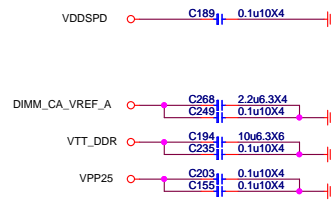
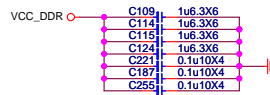
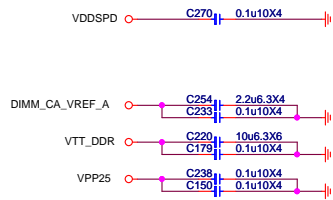
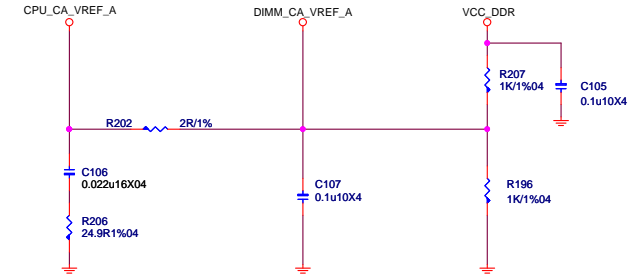
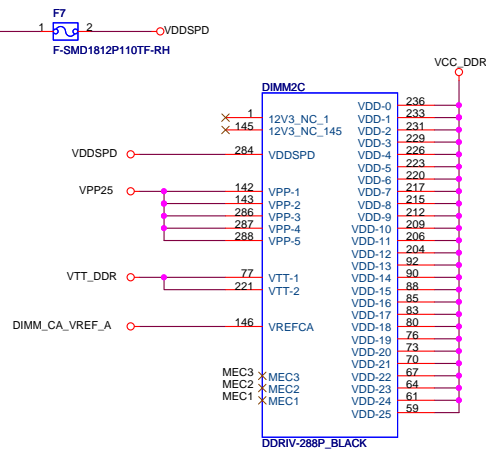
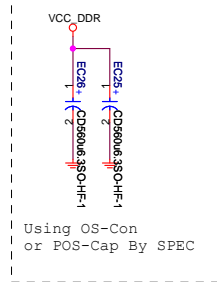


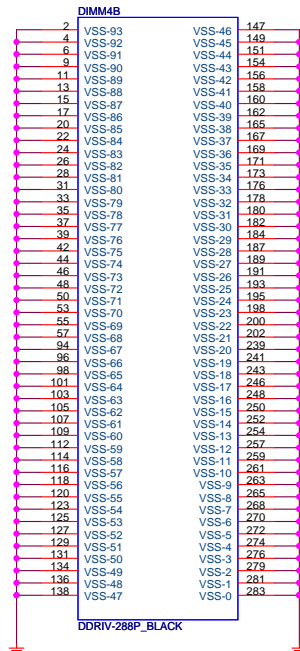
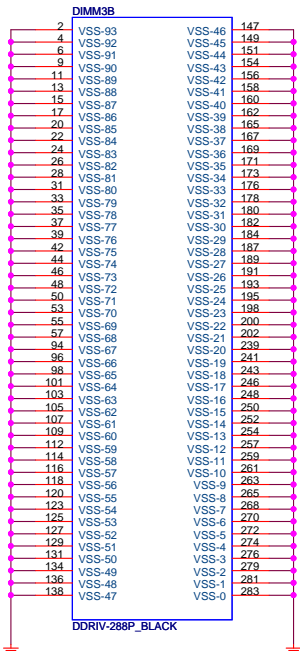
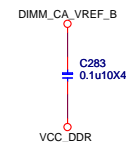
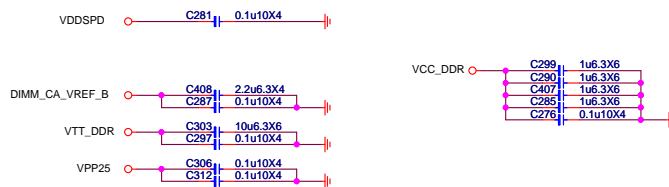
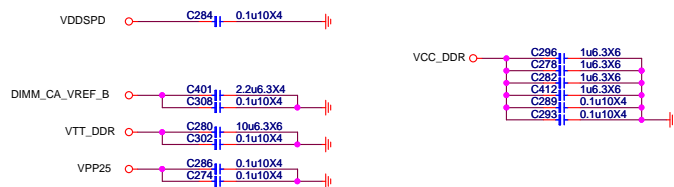
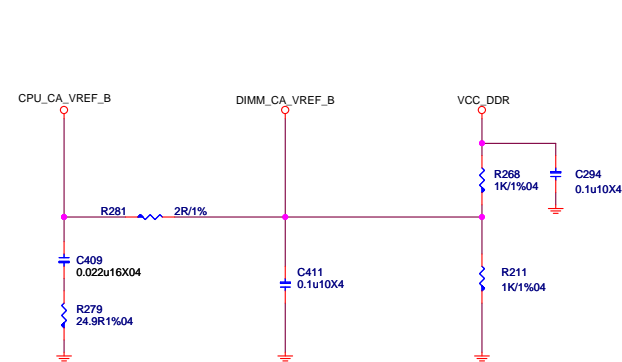
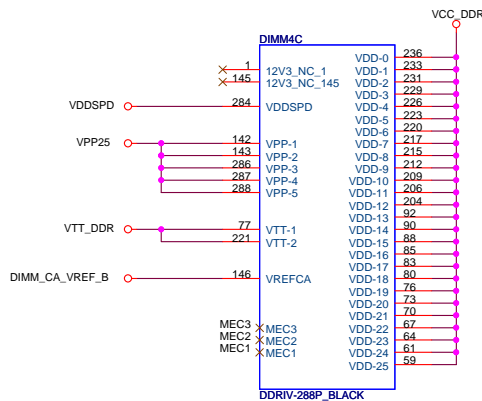
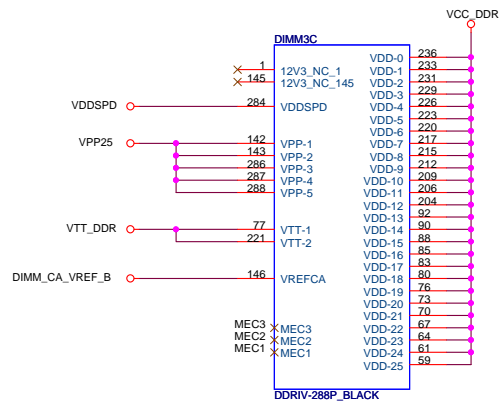




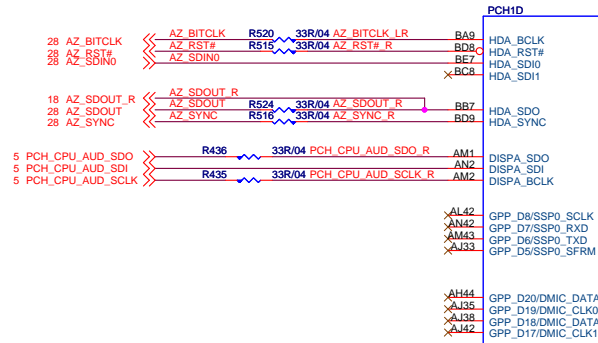
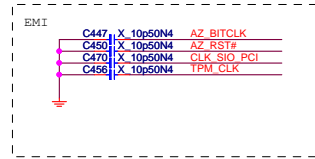


### DIMM SLOT PN BY SPEC





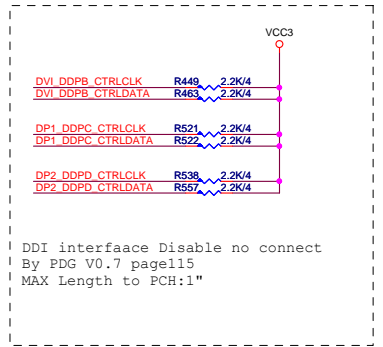




AUDIO

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SPT-H

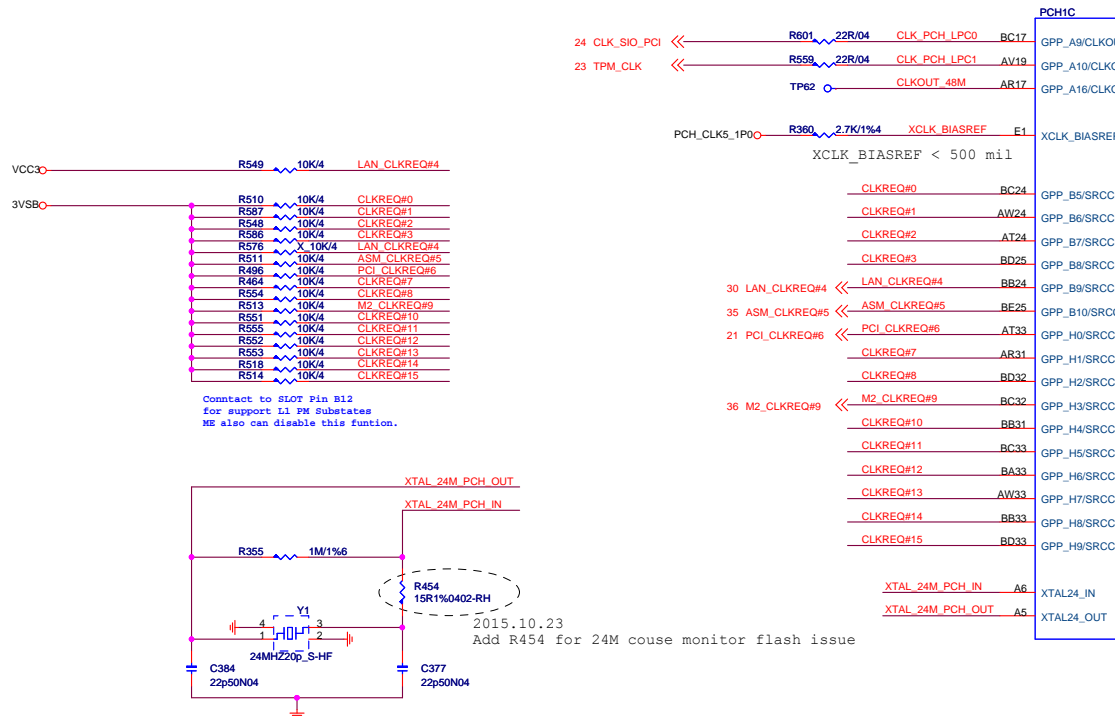


Port B DVI

Port C DisplayPort

Port D DisplayPort

## 24M CLOCK BUFFER Remove



Clock

3 OF 10

SPT-H



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MS-7975

Size

Custom

Document Description

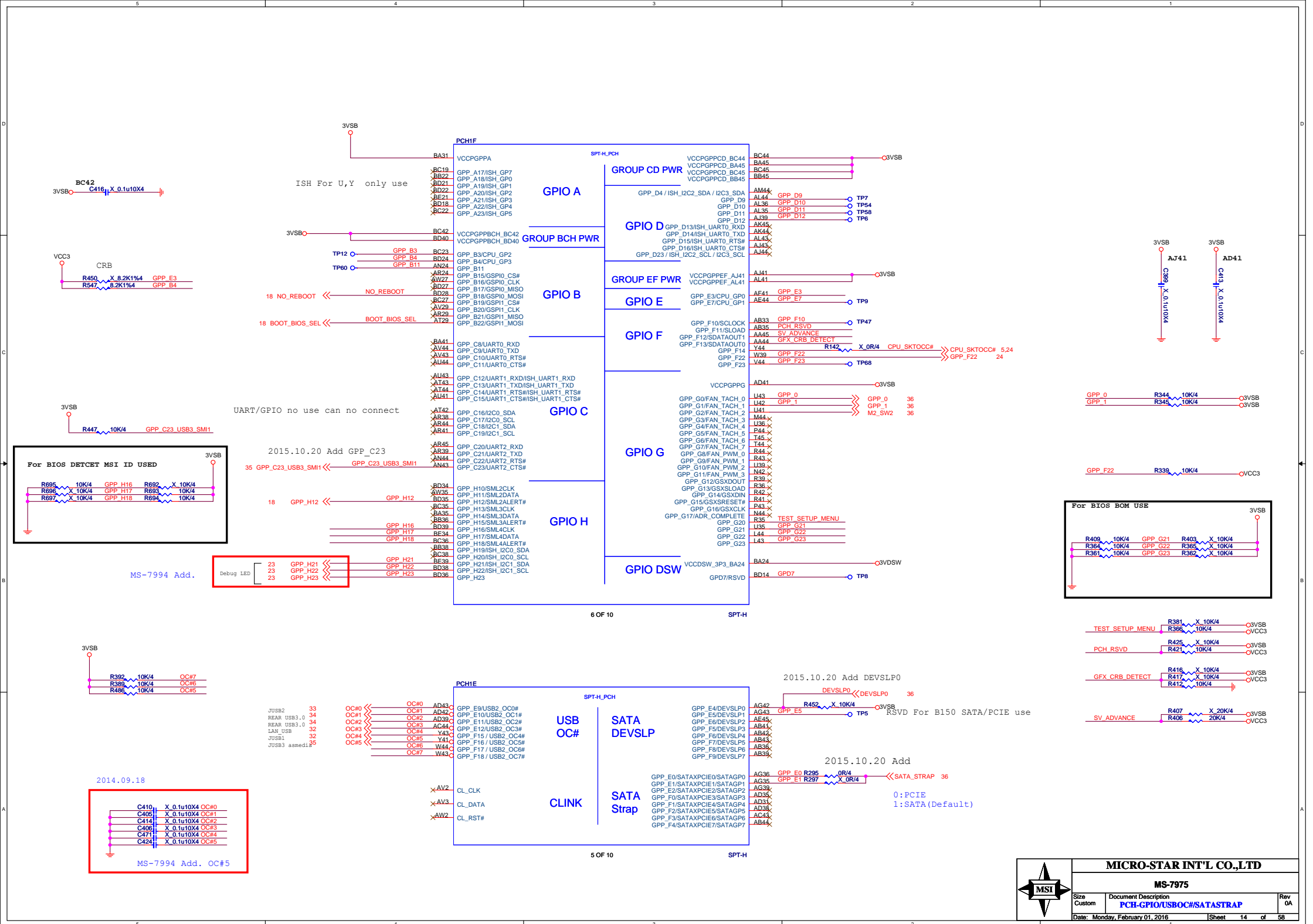
PCH-Audio/Display/Clock

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Rev

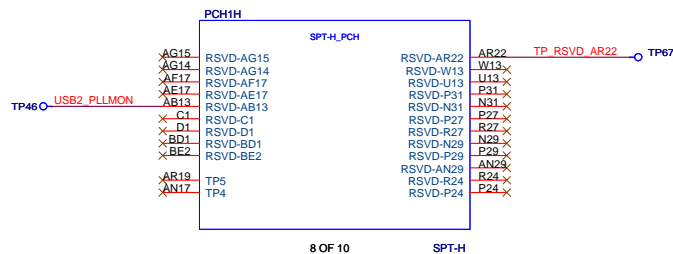
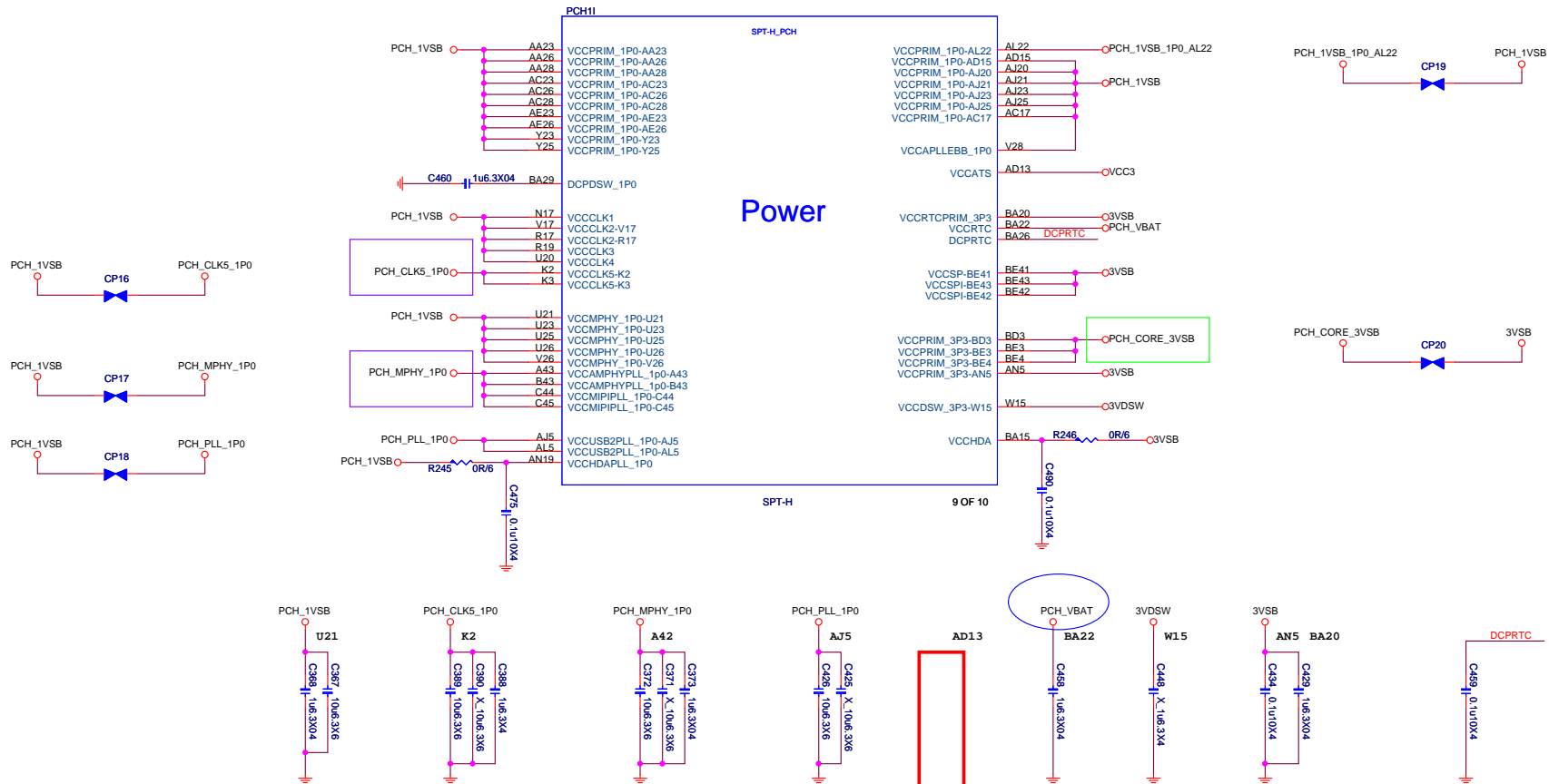
0A





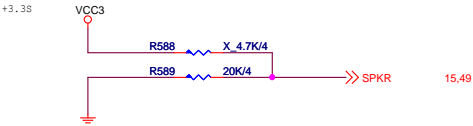






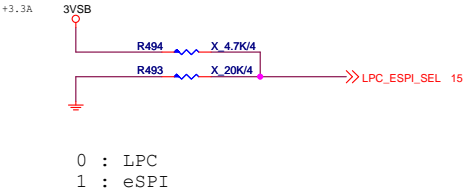


TOP Swap



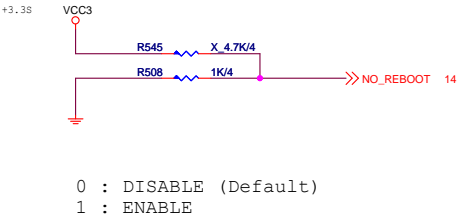
Internal pull-down is disabled after PLTRST#

LPC eSPI Mode



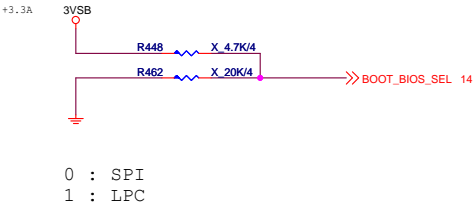
Internal pull-down is disabled after RSMRST

No Reboot



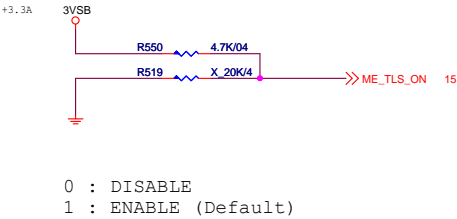
Internal pull-down is disabled after PLTRST#

Boot BIOS



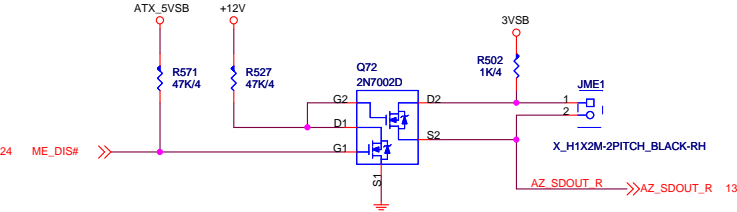
Internal pull-down is disabled after PLTRST

AMT and SBA with confidentiality

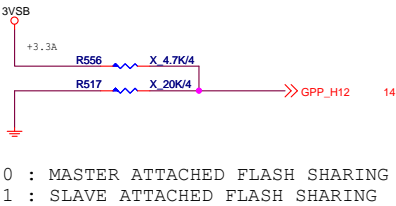


Internal pull-down is disabled after RSMRST

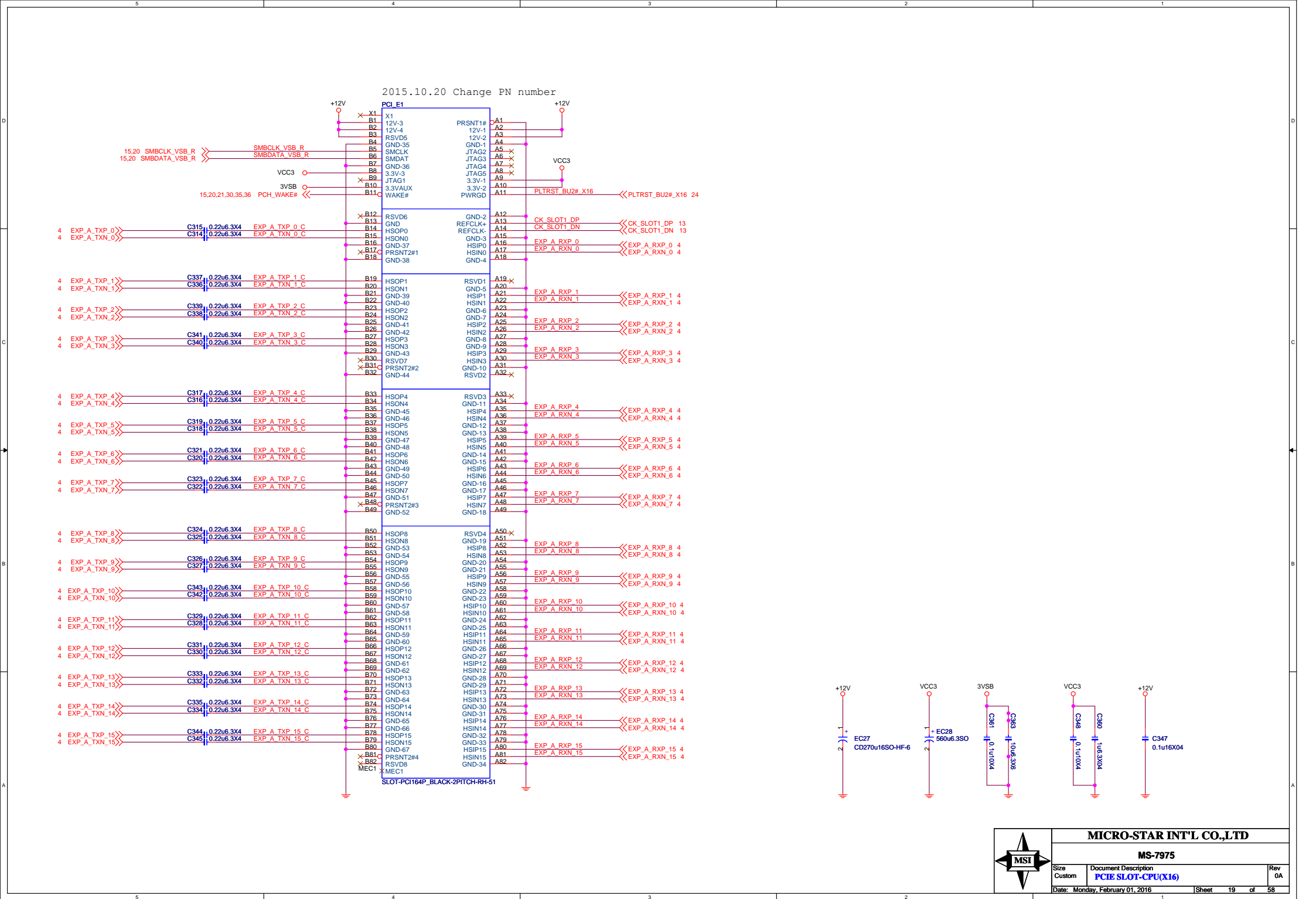
HDA\_SDO



ESPI FLASH SHARING MODE

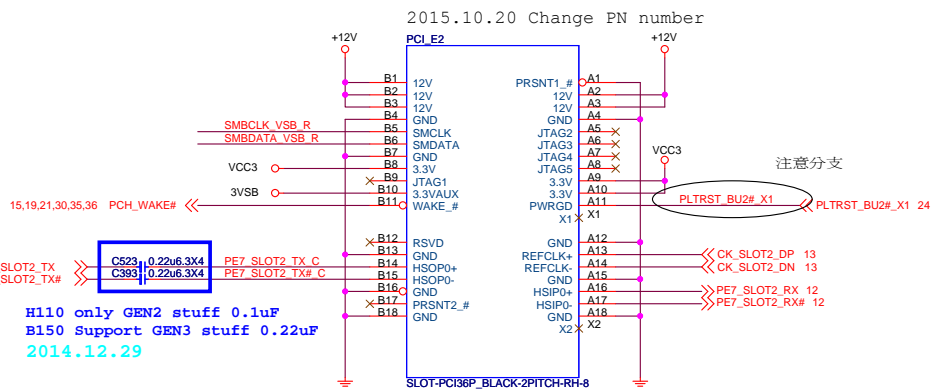


Internal pull-down is disabled after RSMRST



## PCI Express X1 Slot

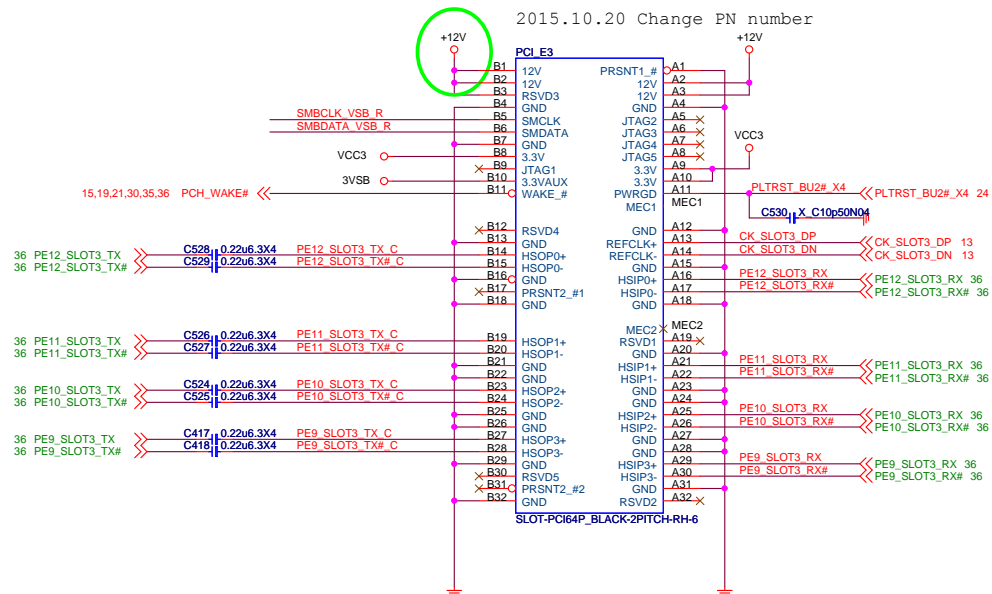
15,19 SMBCLK\_VSB\_R >> SMBCLK\_VSB\_R  
15,19 SMBDATA\_VSB\_R >> SMBDATA\_VSB\_R



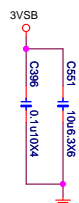
## PCI Express X4 Slot

12V - 2.1A  
VCC3 - 3A  
3VSBV - 375mA

Trace width > 200 mils

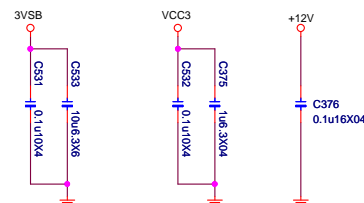


close to slot2



close to slot3

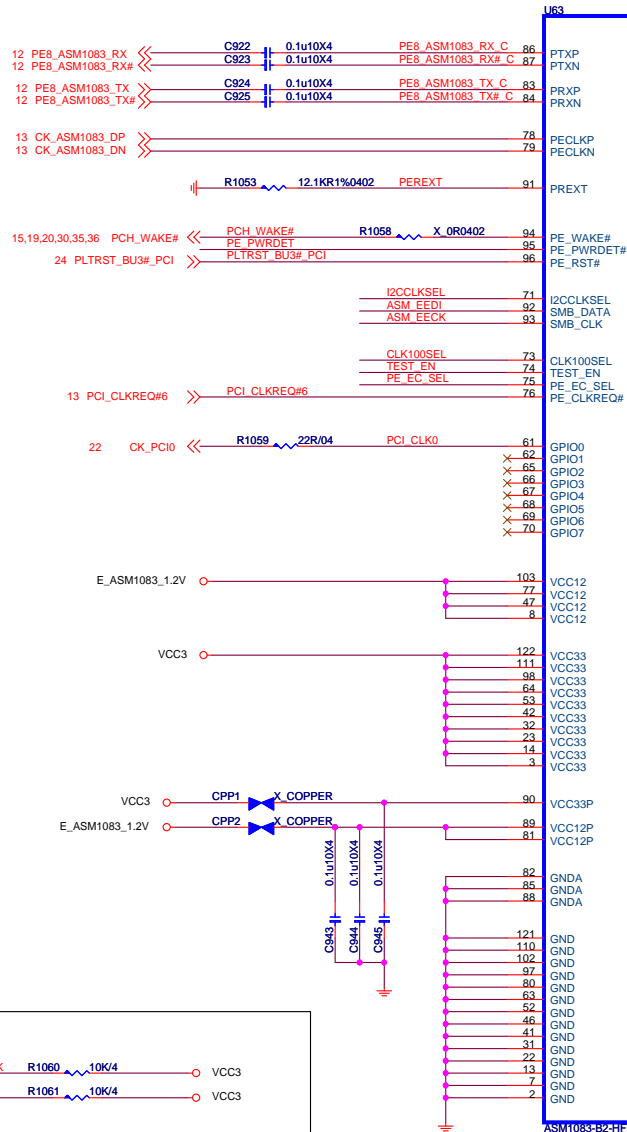
close to slot4



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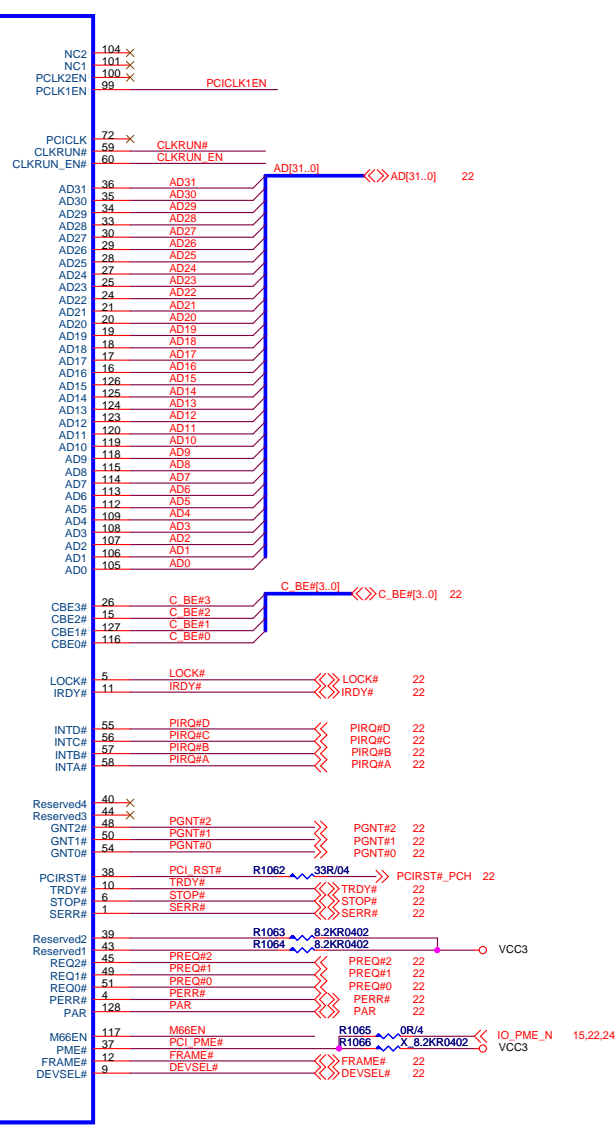
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Size	Document Description	Rev
Custom	PCIE SLOT-PCH(X1)	0A
Date: Tuesday, February 02, 2016	Sheet 20 of 58	

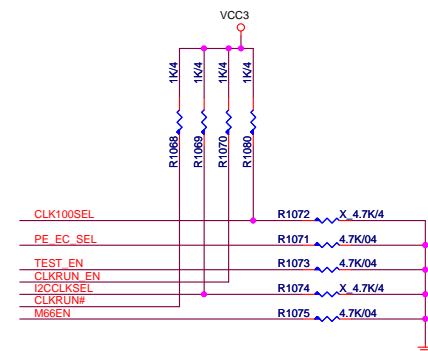


ASM1083

ASM1083-B2-HF



## H/W Strapping



CLK100SEL-  
"H" for PECLK input only  
"L" for PECLK & PCICLK input

PE\_EC\_SEL-  
"H" for Express Card mode  
"L" for PCIe Riser Card mode

TEST\_EN-  
"H" for Test Mode Enable  
"L" for Test Mode Disable

CLKRUN\_EN-  
"H" for CLKRUN Mode Disable  
"L" for CLKRUN Mode Enable

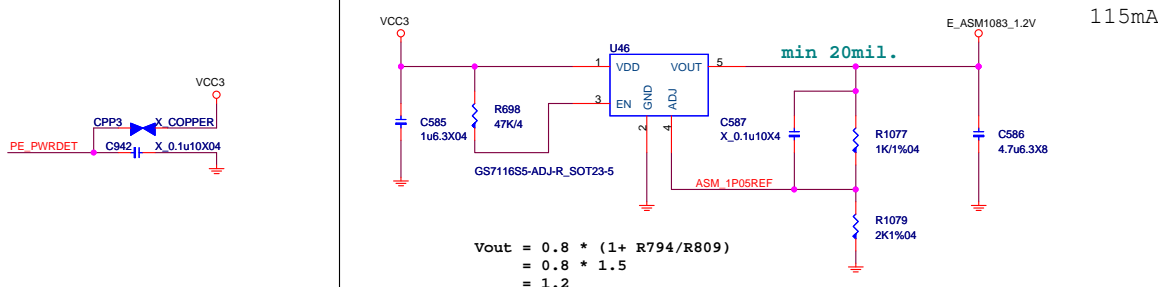
I2CCLKSEL-  
"H" is 135KHz I2CCLK  
"L" is 67.5KHz I2CCLK



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Custom	ASM1083 PCI Brl.	0A
Date: Monday, February 01, 2016	Sheet 21 of 58	



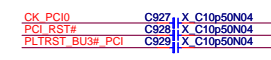
$$V_{out} = 0.8 * (1 + R_{794}/R_{809})$$

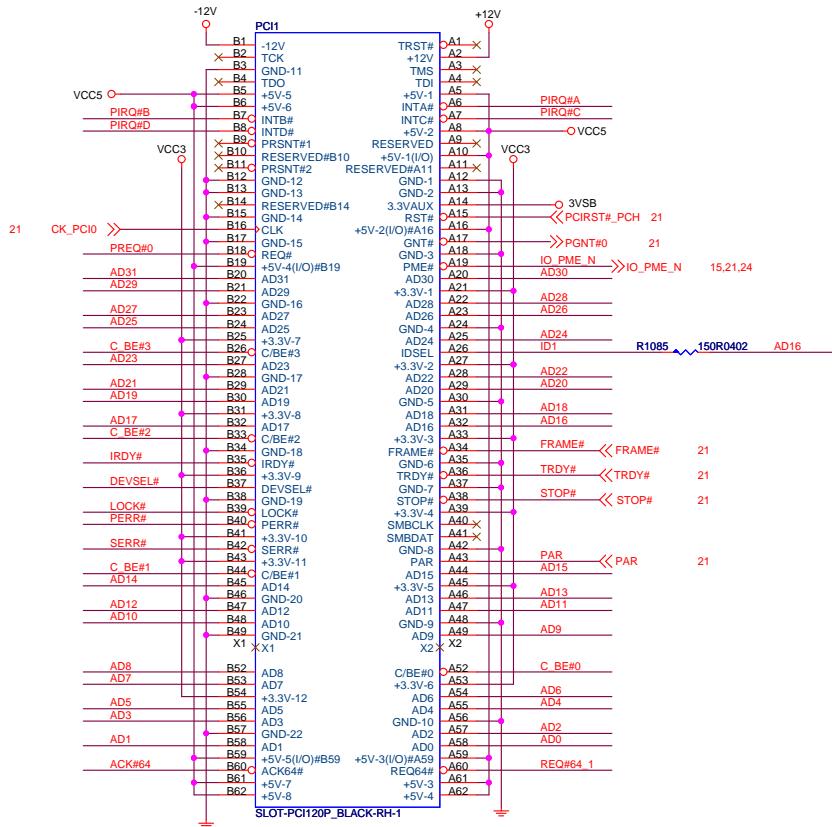
$$= 0.8 * 1.5$$

$$= 1.2$$

115mA

EMI

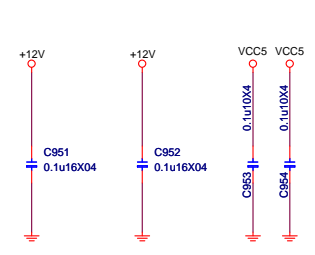
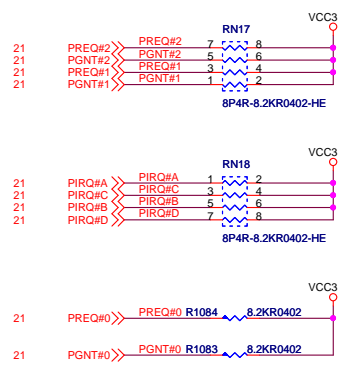
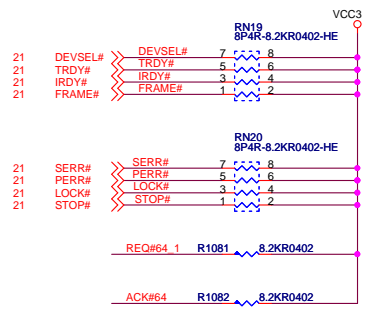
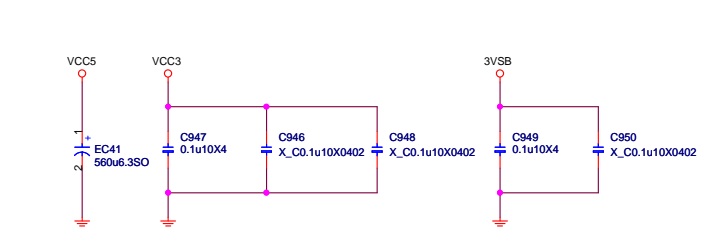




**IDSEL = AD16**  
**MASTER = PREQ#0**  
**PIRQ#A**

AD[31..0] <<> AD[31..0] 21  
 C\_BE#[3..0] <<> C\_BE#[3..0] 21

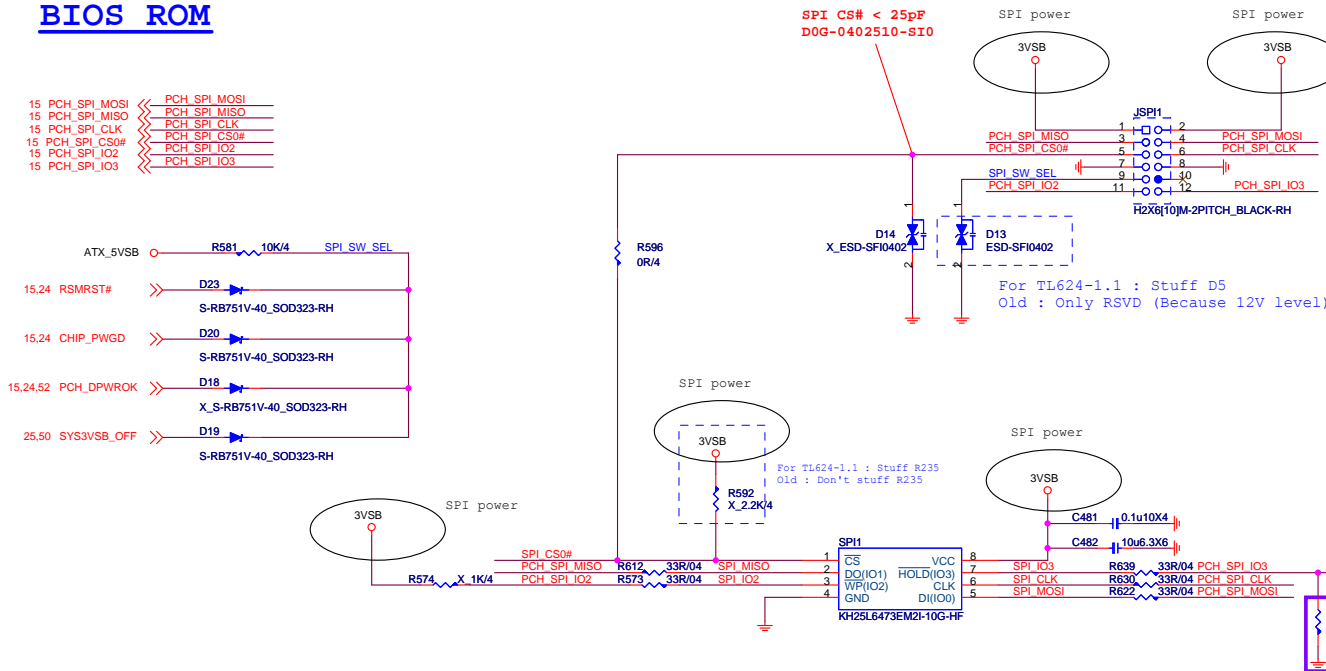
### PCI PULL-UP / DOWN RESISTORS



	<b>MICRO-STAR INT'L CO.,LTD</b>		
	<b>MS-7975</b>		
	Size Custom	Document Description <b>PCx1 Slots</b>	Rev 0A
Date: Monday, February 01, 2016		Sheet 22 of 58	



## BIOS ROM

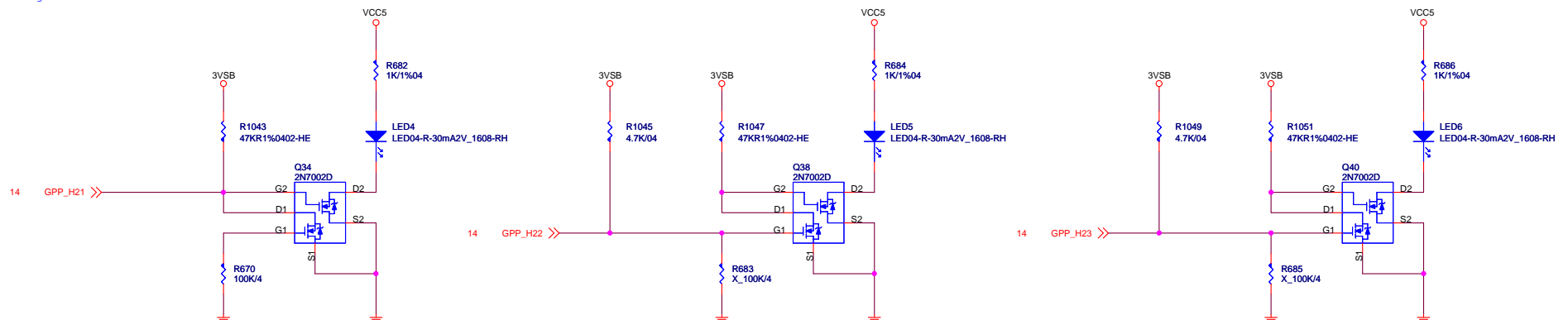


\* if you support Standby power in S5 Status(Ex; PCH is B75 Chipset) , component Q23.G Pull-high to ATX\_5VSB , Q23 must select "Vth" under 1V (Component Suggestion as below )

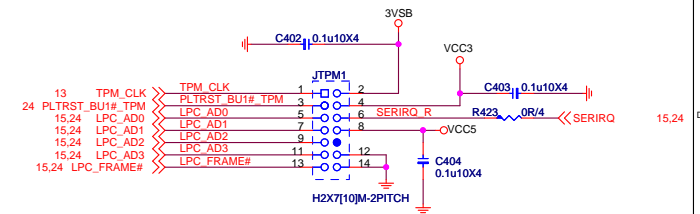
D03-0341409-A68 / D03-0230019-A30

## Debug LED

MS-7994 Add. Debug LED circuit



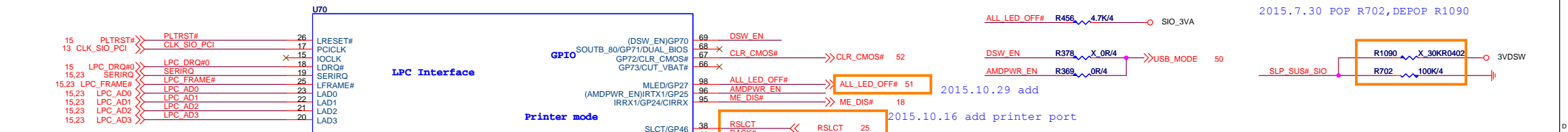
## TPM



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Size Custom	Document Description <b>BIOS ROM/TPM/Debug LED</b>	Rev 0A
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POWER ON STRAPPING PIN FOR NCT6792					
PIN	6792 NAME	Circuit NAME	0	1	Strap Point
9	UARTA_P80_EN	RTSB#	DISABLE UARTA80	ENABLE UARTA80	LRESET
10	UARTB_P80_EN	DTRB#	DISABLE UARTB80	ENABLE UARTB80	LRESET
12	TEST1MODE_EN	TEST1MODE	DISABLE TEST1MODE	ENABLE TEST1MODE	LRESET
31	2E_4E_SEL	RTSA#	I/O ADDRESS 2E	I/O ADDRESS 4E	LRESET
32	24_48_SEL	DTRA#	24M CLOCK SOURCE	48M CLOCK SOURCE	INTERNAL PWROK
34	P80_EN	SOUTA	ENABLE Non_PORT80	ENABLE PORT80	LRESET
62	TESTMODE_EN	SLP_S5_LCH#	DISABLE TESTMODE	ENABLE TESTMODE	INTERNAL RSMRST
69	DSW_EN	DSW_EN	DISABLE INTEL DSW	ENABLE INTEL DSW	INTERNAL RSMRST
96	AMDPWR_EN	AMDPWR_EN	DISABLE AMD PWR SEQ	ENABLE AMD PWR SEQ	INTERNAL RSMRST

**Note:**  
If PIN34 strapping low, BIOS must programming LPT or GPIO

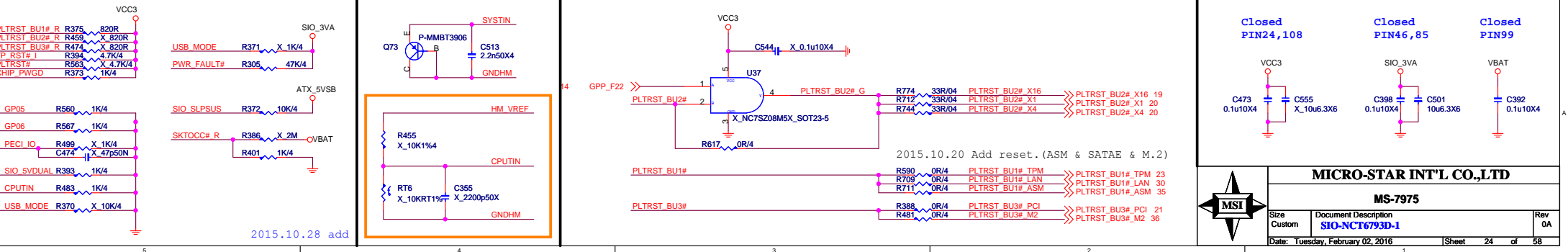
### 3V Analog Power

2015.7.30 remove R438,R452

6792 SLP\_S5\_LCH# pull down  
VIN8 pull down  
AVCC3 = VCC3

6793 SLP\_S5\_LCH# pull down and stuff 4.7uf  
VIN8(WDT#) pull down  
AVCC3 = SIO\_3VA

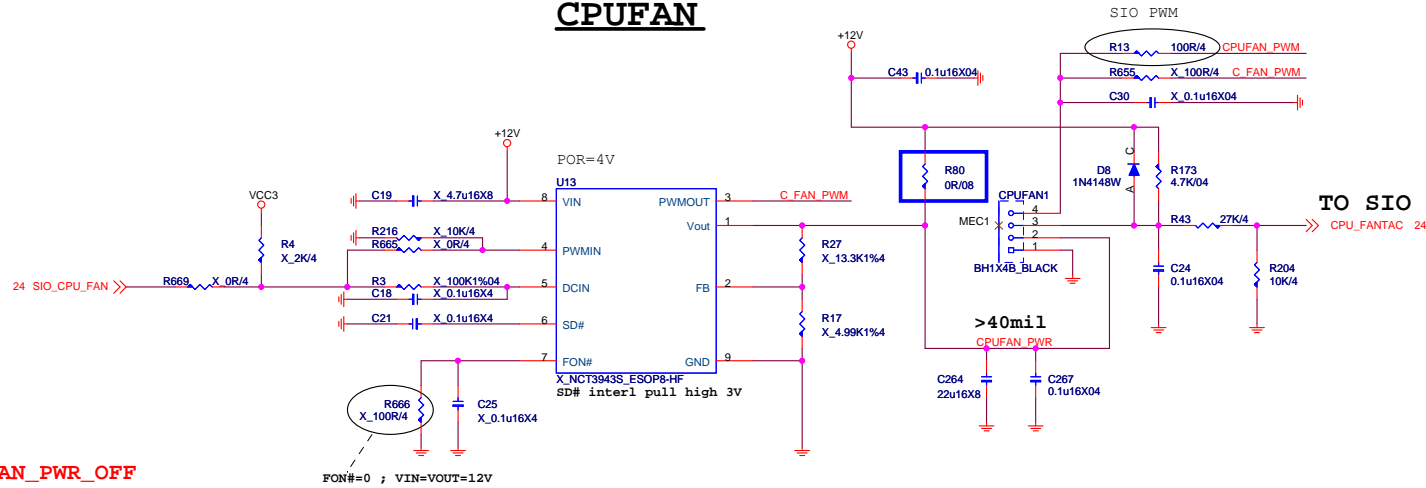
6792 Co-lay 6793





Type G : 4 PIN CPU FAN USE SIO PWM (Reserve NCT3943S & WITHOUT CUT POWER)

CPUFAN



CPUFAN\_PWR\_OFF

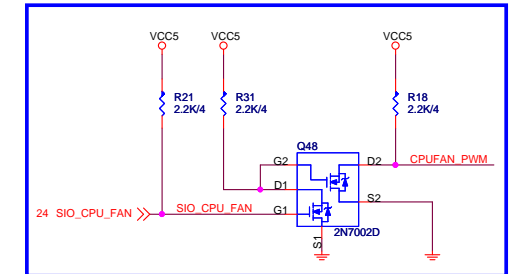
## GPIO Control

## Default GPI

If USE CUT POWER

1.OPEN DRAIN LOW:SD# LOW Active , CPUFAN(PIN2)= 0V

**2.OPEN DRAIN : SD# Internal Pull high , CPUFAN(PIN2)=12V**

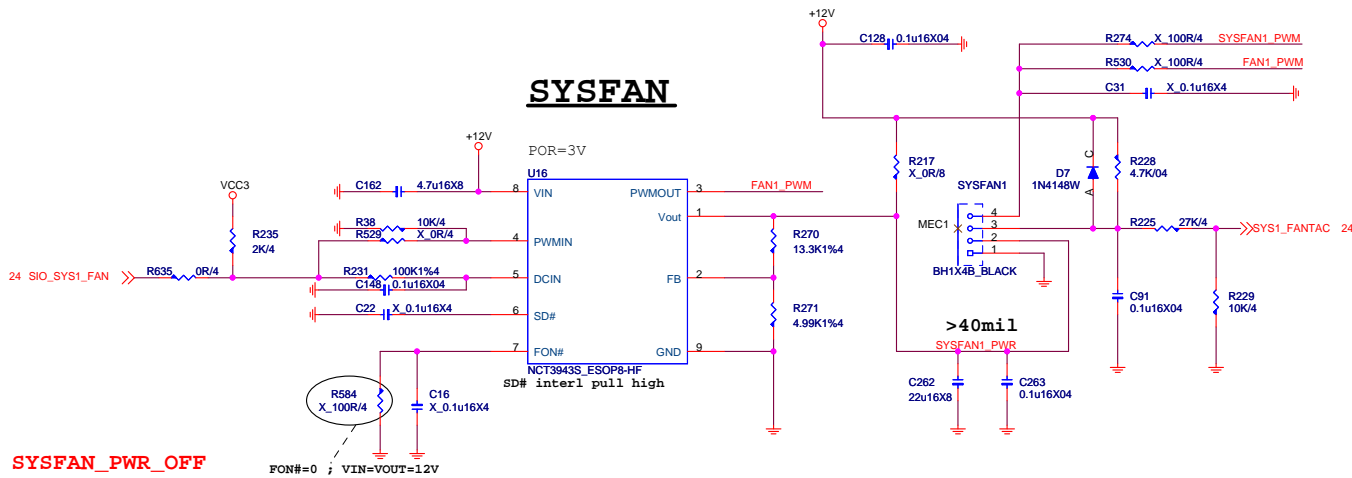


**MICRO-STAR INT'L CO.,LTD**

MS-7975

Size Custom	Document Description <b>CPU FAN Controller</b>	Rev 0A
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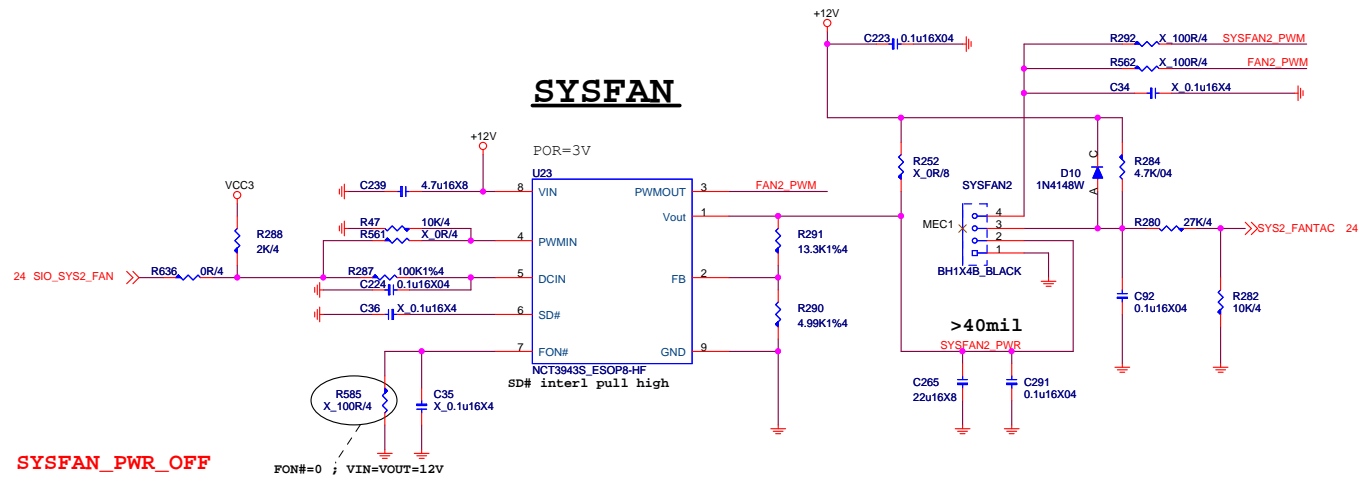
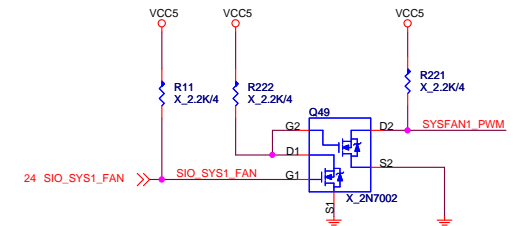
Type H : 4/3 PIN SYS FAN FROM NCT3943S(USE SIO CUT POWER)



```

SYSFAN_PWR_OFF          FON#=0 ; VI
SIO control
Close SIO_SYS1_FAN Vout=0

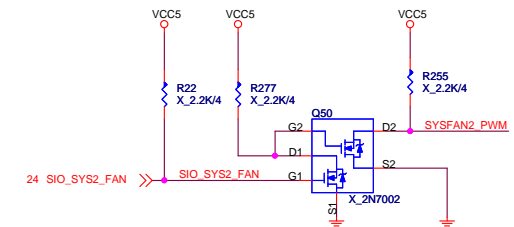
```



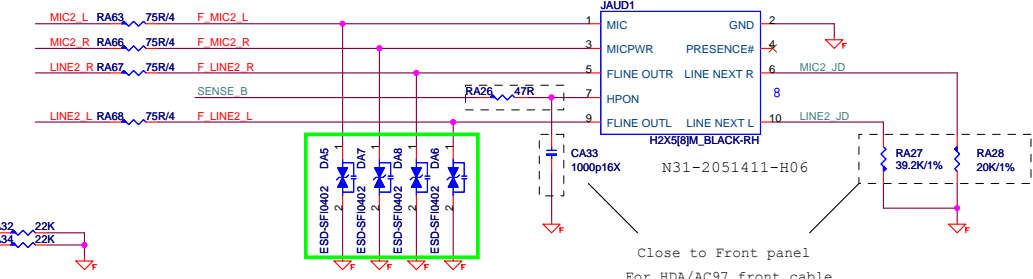
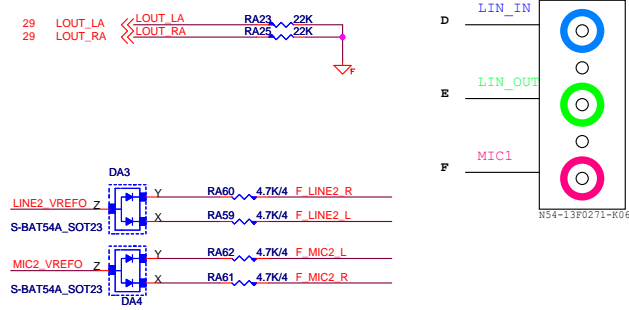
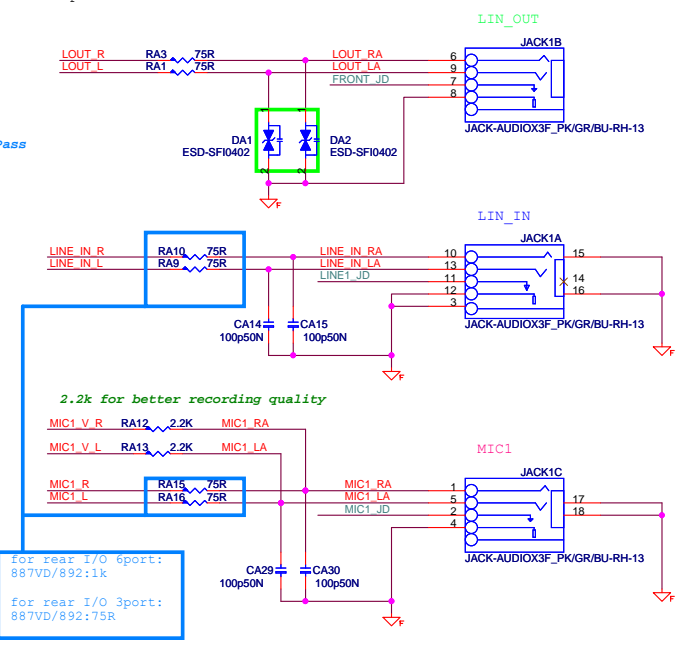
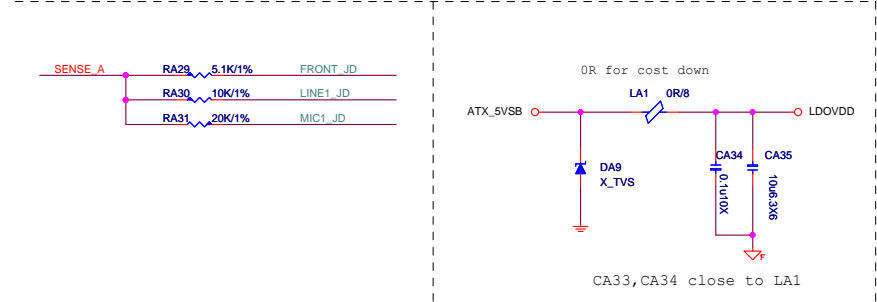
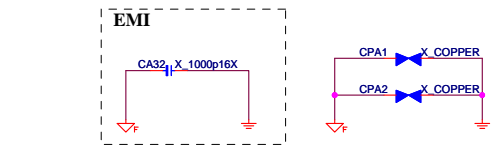
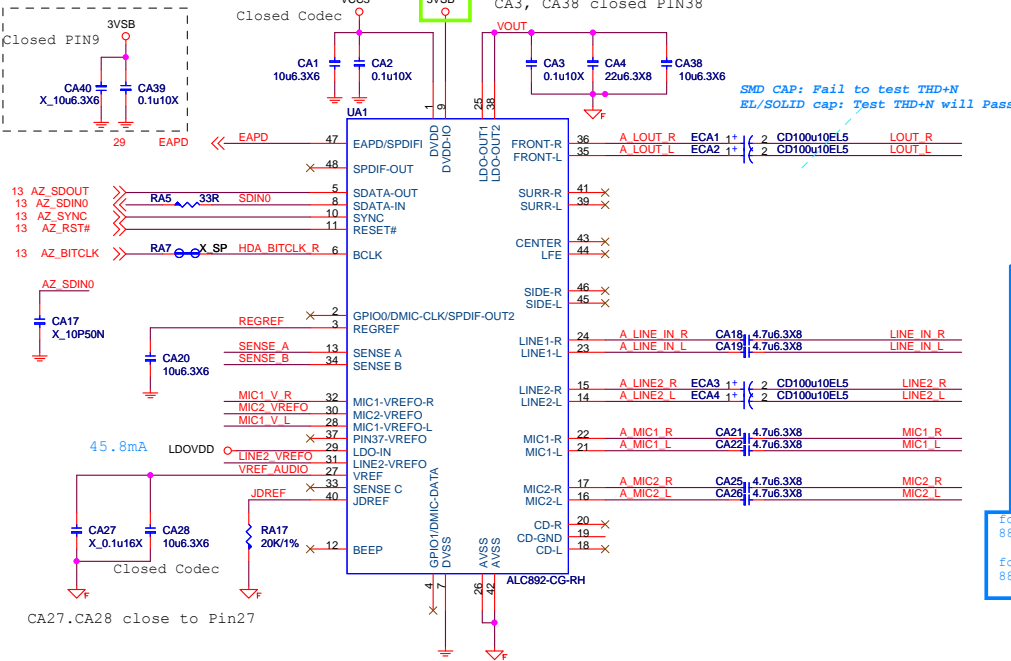
```

SYSFAN_PWR_OFF          FON#=0 ; VI
SIO control
Close SIO_SYS1_FAN Vout=0

```



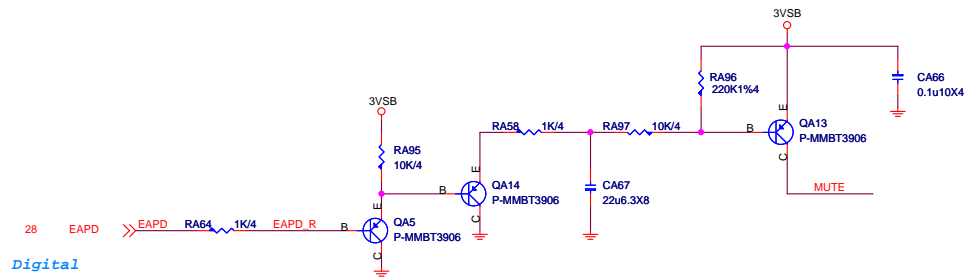
Type B:  
ALC892/887



Varister --> cap for cost down  
DOG-2950500-SI0  
DOG-3010510-I05  
Close to Jack

MSI			
MICRO-STAR INT'L CO.,LTD			
MS-7975			
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**Rear Line OUT De-POP circuit**  
(De-pop circuit for Rear Line out & Front Headphone out)

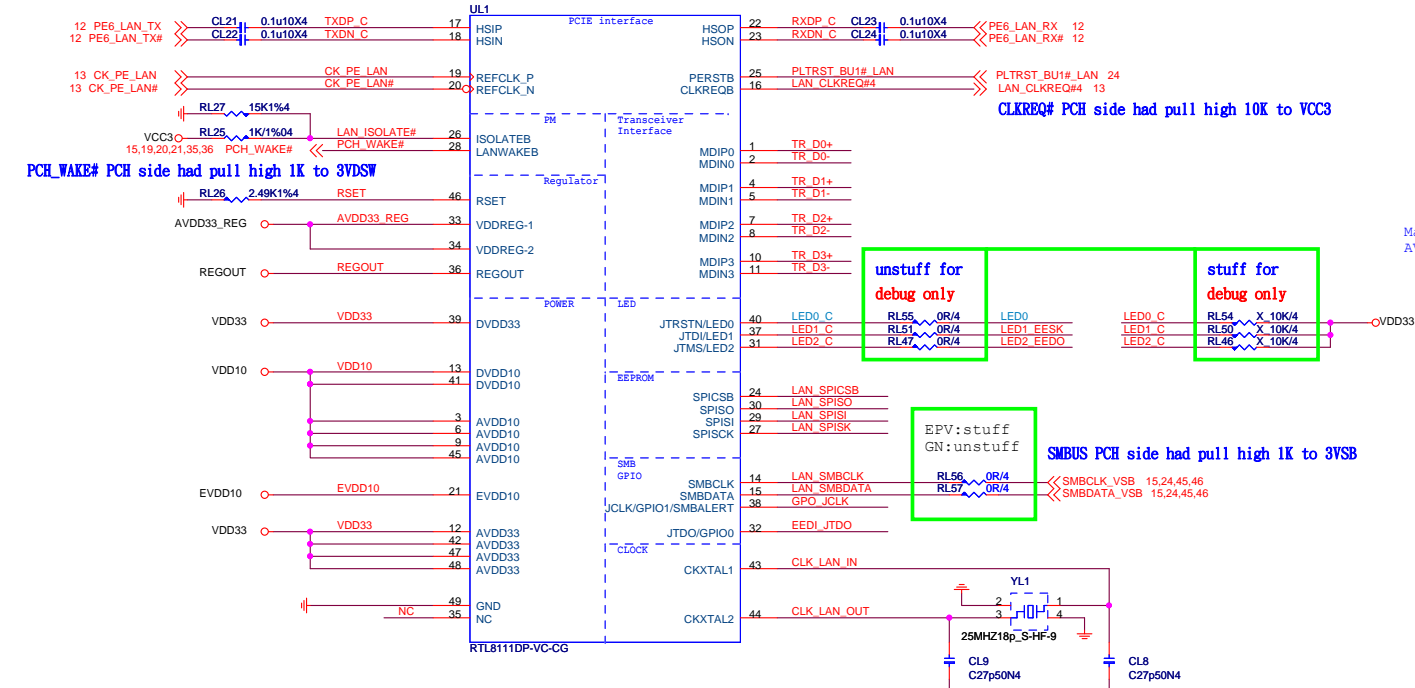


Analog

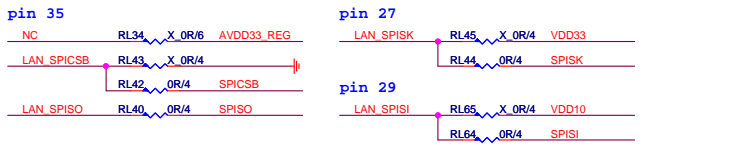
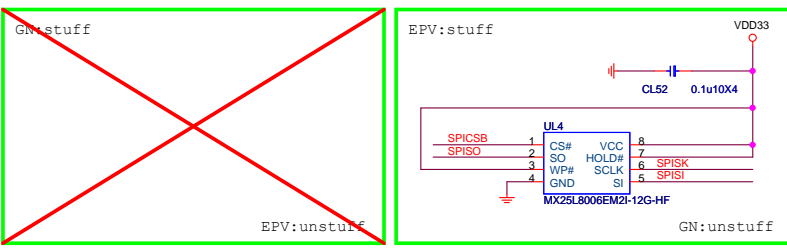
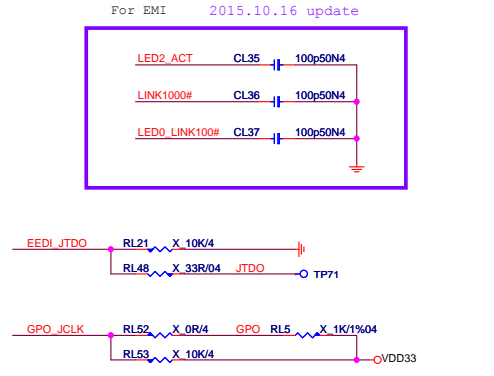
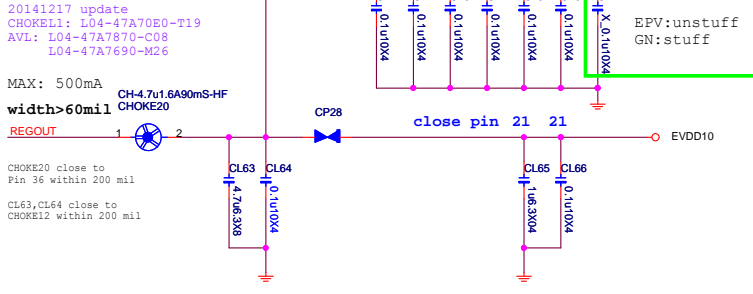
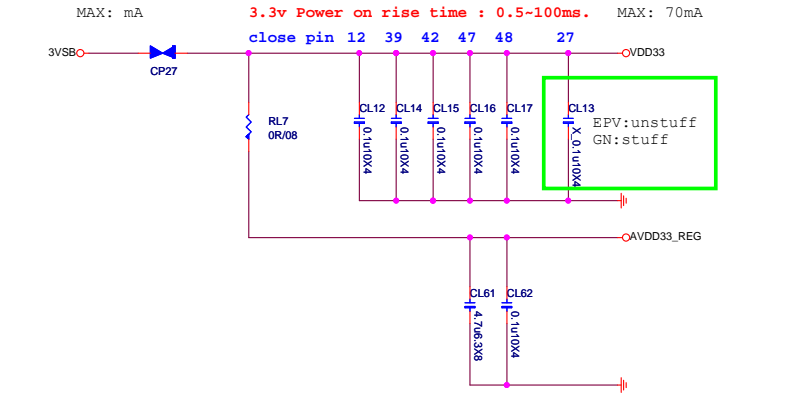
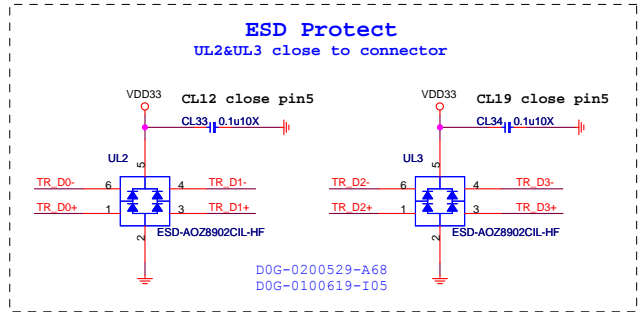
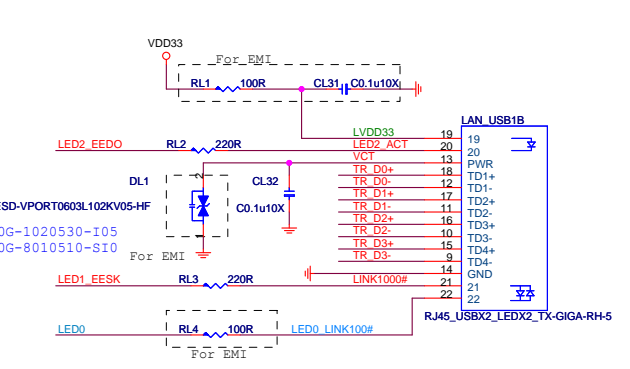




RTL8111EPV(default) coly RTL8111GN Giga LAN



LAN Connector



Configuration Table	RL34	RL43	RL42	RL41	RL40	RL45	RL44	RL65	RL64
8111GN	O	O	X	X	X	O	X	O	X
8111EPV (default)	X	X	O	O	O	X	O	X	O

Configuration Table	RL21	RL48	RL53	RL52
8111GN	O	X	X	O
8111EPV (default)	X	X	X	X
8111EPV (debug only)	X	O	X	O

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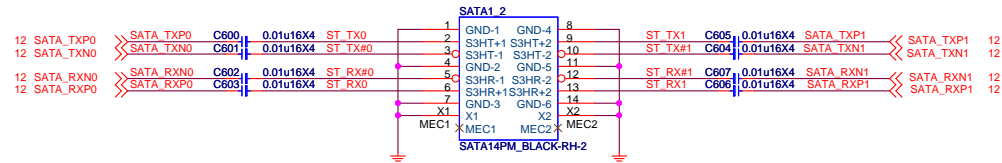
Size Custom Document Description **LAN - Intel I219V** Rev 0A

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## SATA 6G PORT 0,1

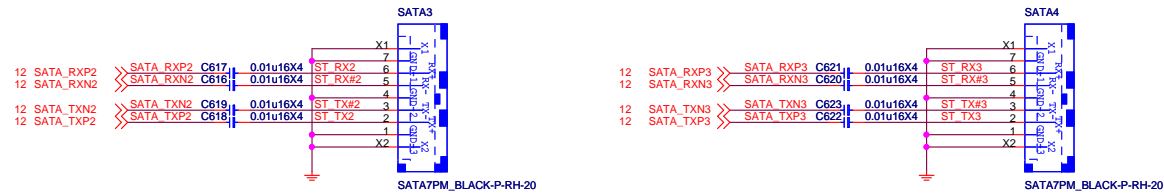
2015.10.20 Add SATA

3.0 Black 90 degree



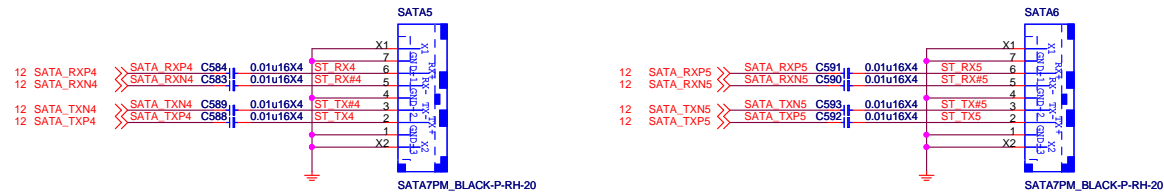
## SATA 6G PORT 2,3

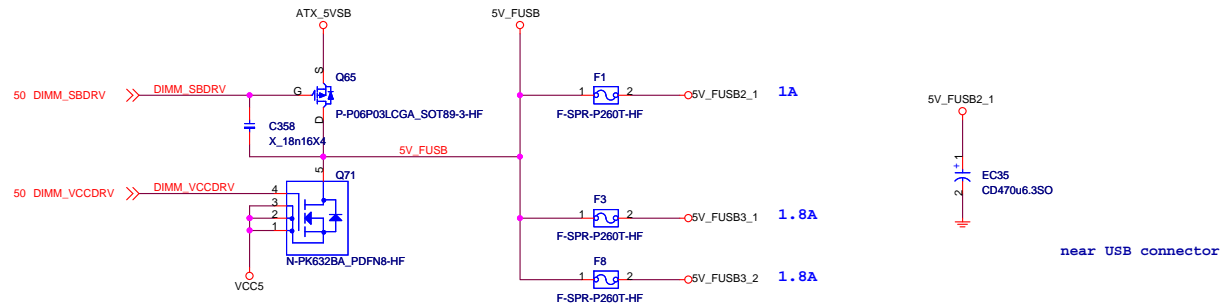
3.0 Black 90 degree



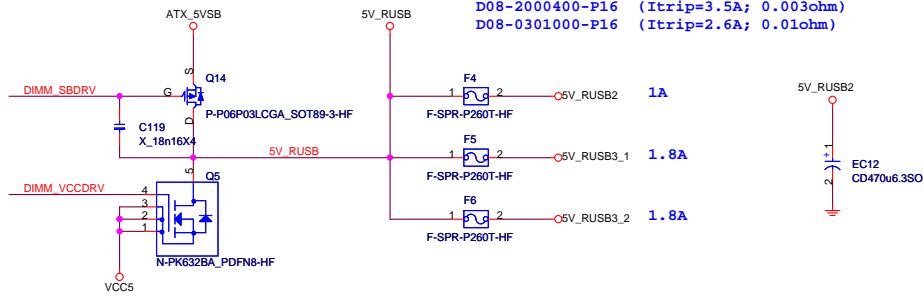
## SATA 6G PORT 4,5

3.0 Black 90 degree



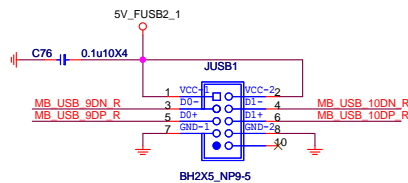
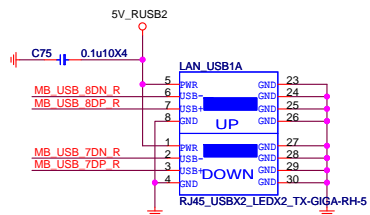
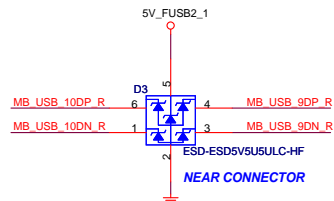
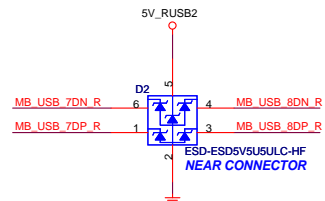
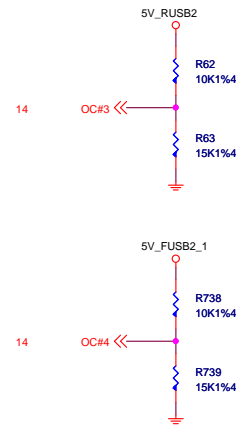
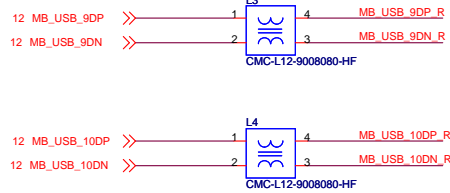
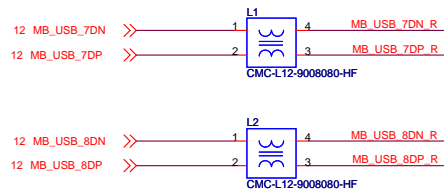


D08-2000400-P16 (Itrip=3.5A; 0.003ohm)  
D08-0301000-P16 (Itrip=2.6A; 0.01ohm)

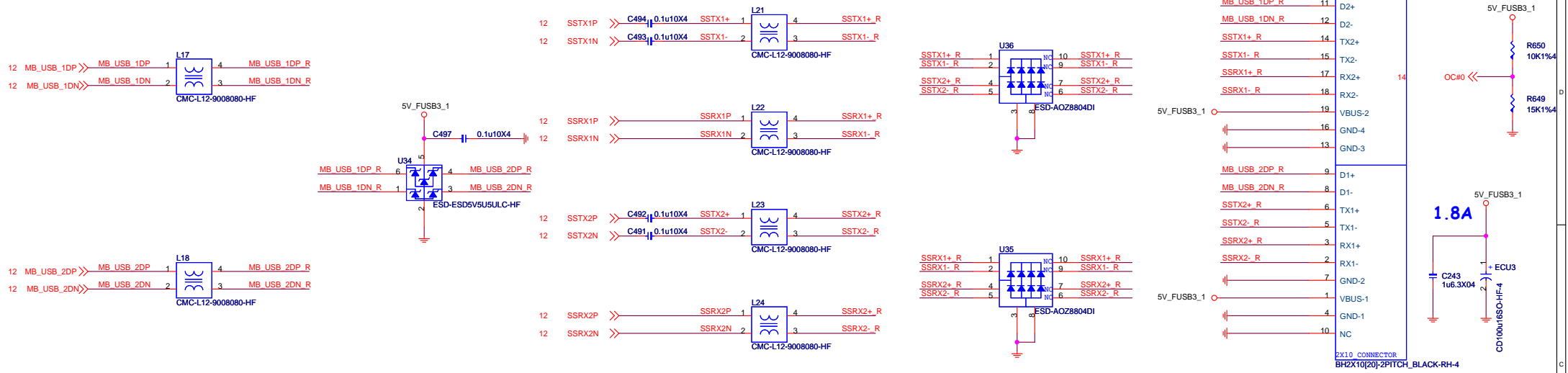


#### REAR USB PORT 7,8 (OC3#)

#### FRONT USB PORT 9,10 (OC4#)



### FRONT USB3.0 (OC0#)

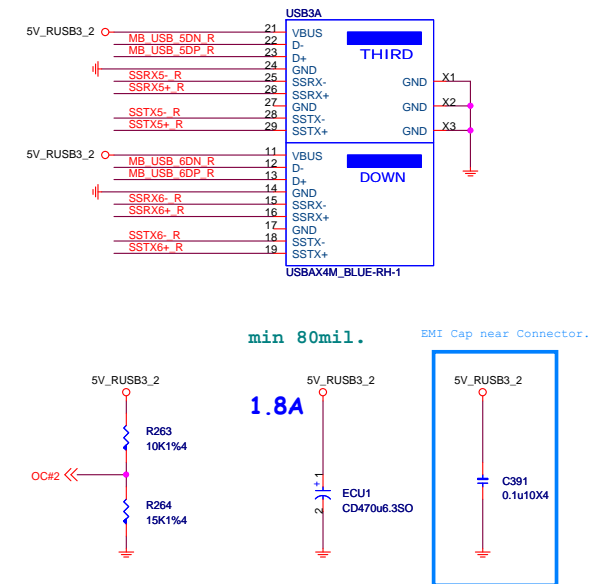
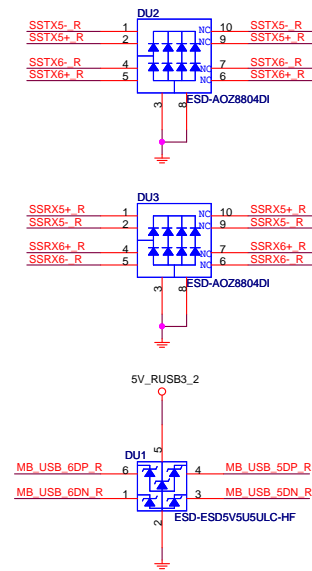
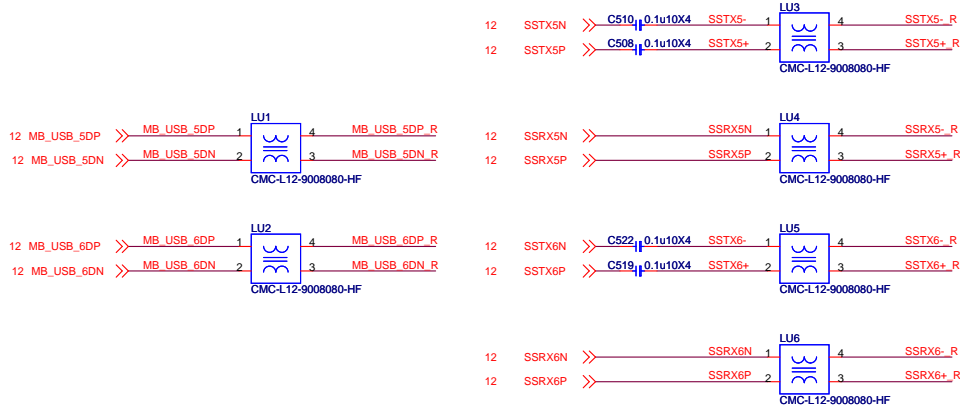


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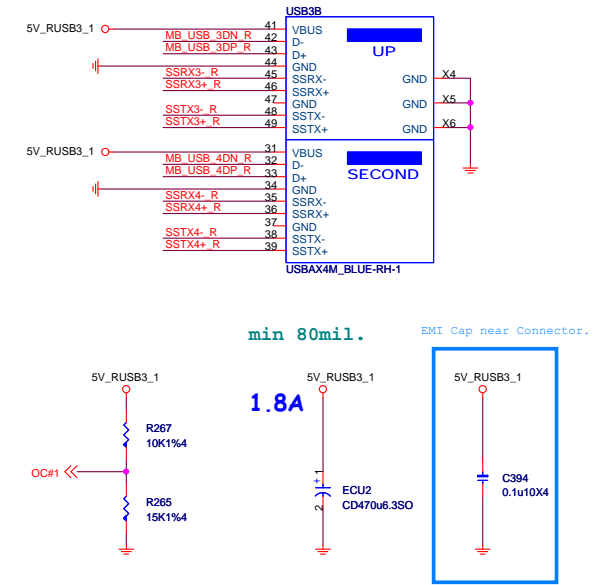
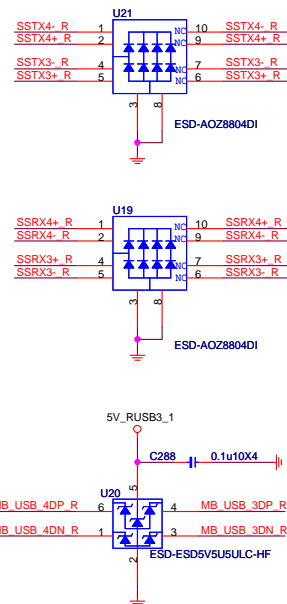
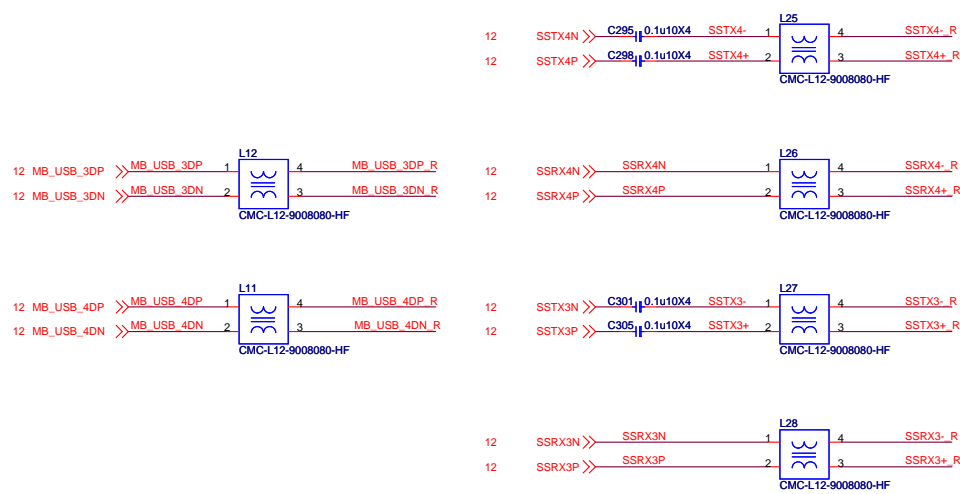
**MS-7975**

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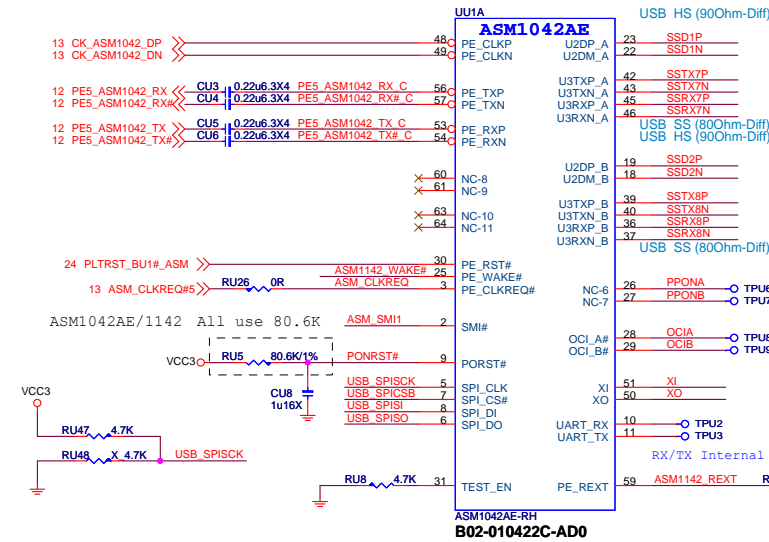
## REAR USB3.0 (OC2#)



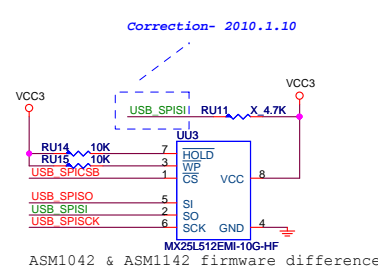
## REAR USB3.0 (OC1#)



## ASM1042 USB3.0



## EEPROM

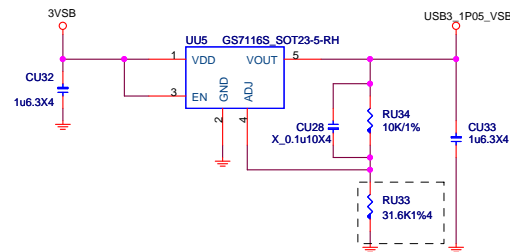


Layout Guide:

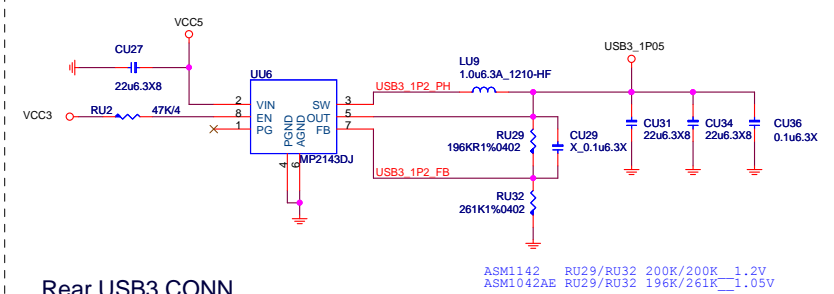
- 1.) USB3.1 to Connector Total Length < 1.5"
- 2.) VIA hole < 2

UREXT,PEUREXT(W/S): 10/7  
OCIA,OCIB,PPONA,PPONB(W/S): 5/8  
X0/XI (95hm-Diff,Spacing 30mil)

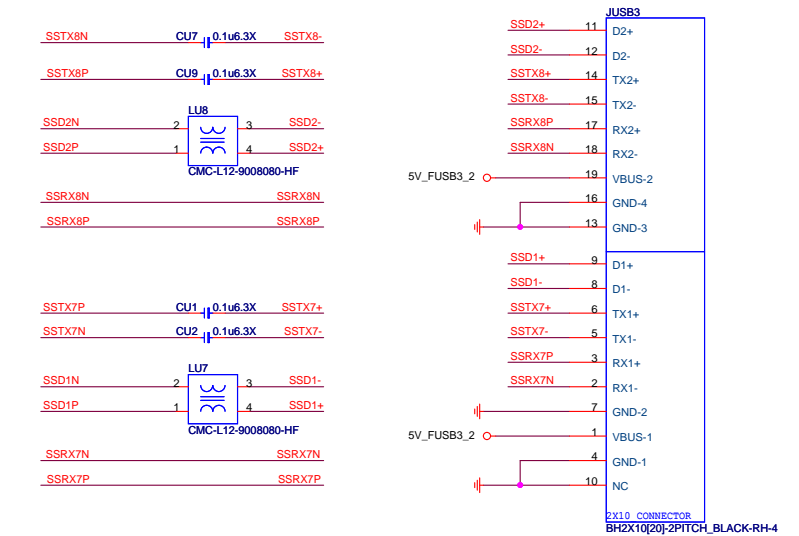
## ASM1142 1.05 VSB Power



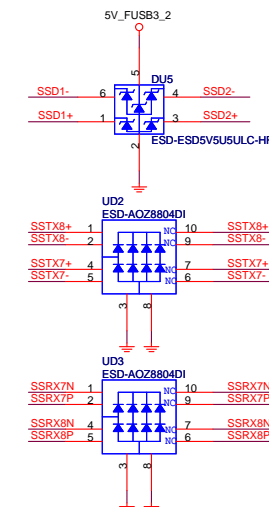
## ASM1042 1.05 Power



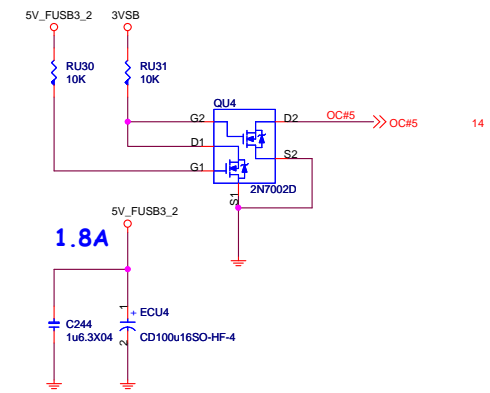
## Rear USB3 CONN



## ESD Protection NEAR CONNECTOR

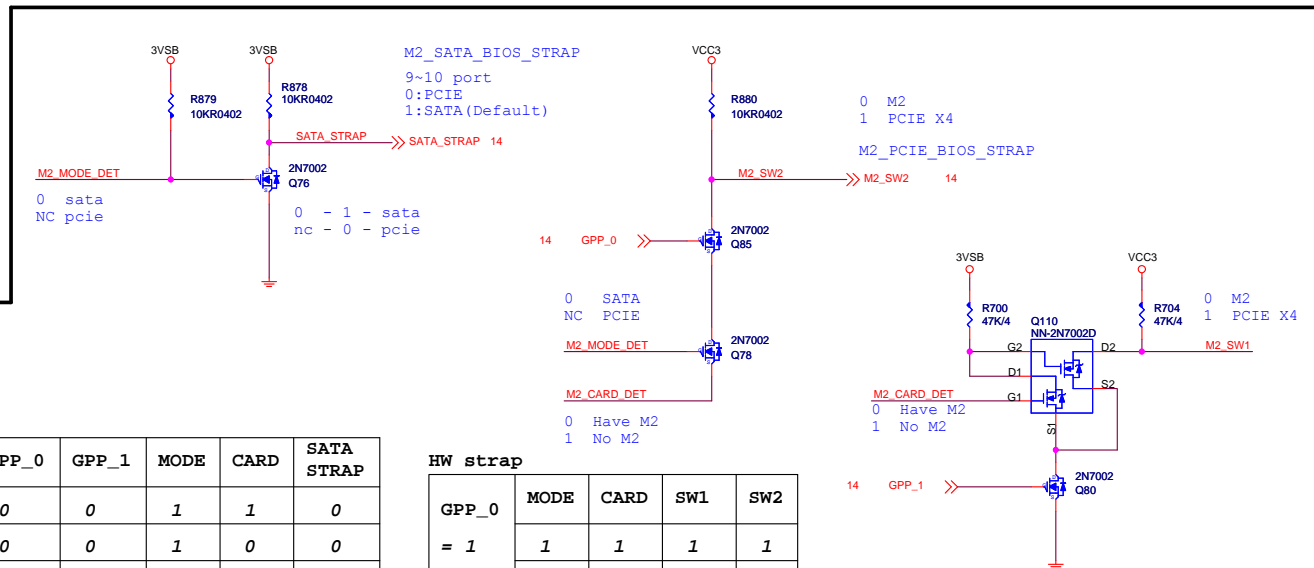
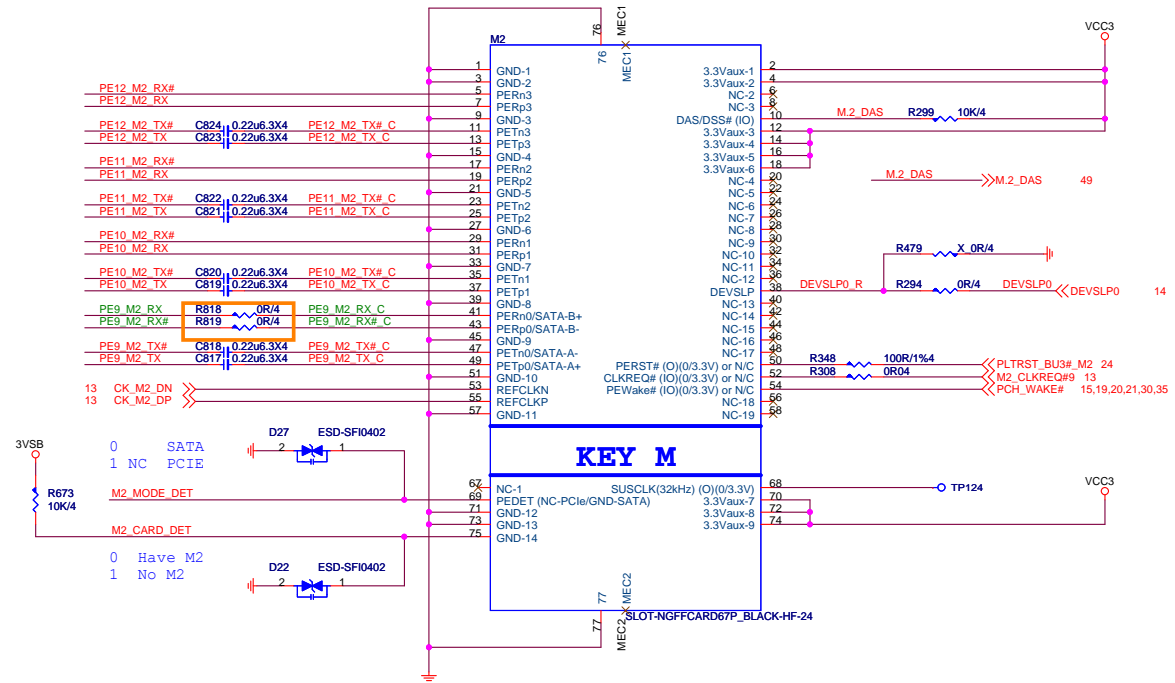
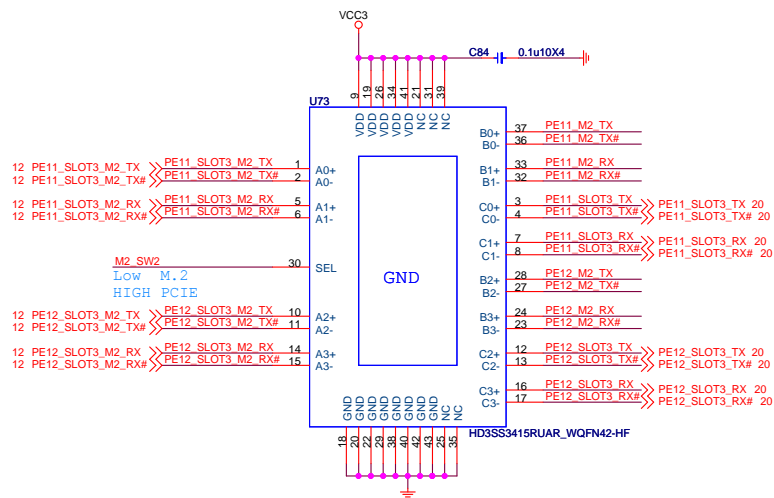
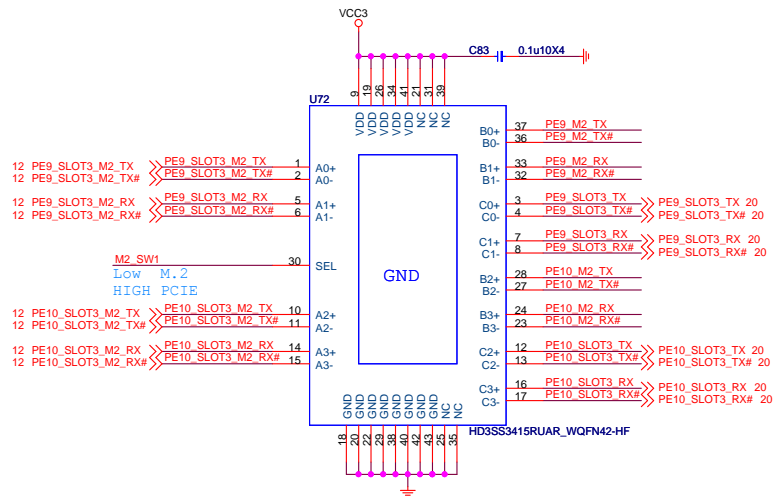


## OC

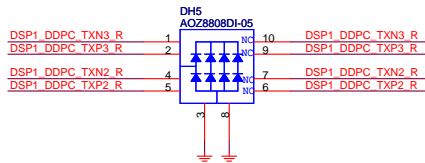
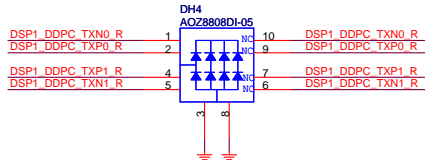
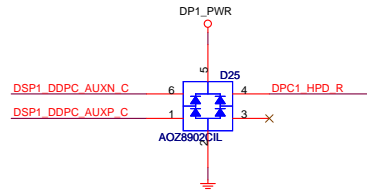


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Date: Wednesday, February 03, 2016		Sheet	35 of 58

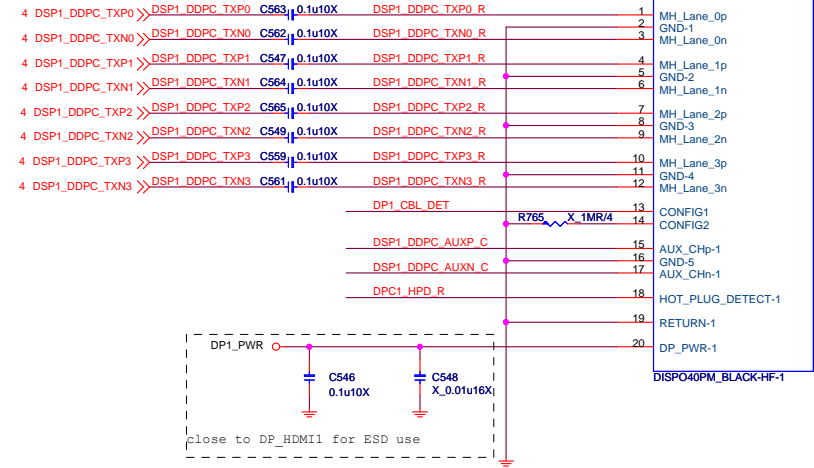
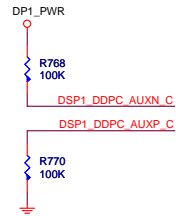
2015.11.11  
If only SATA, change to 0.01u



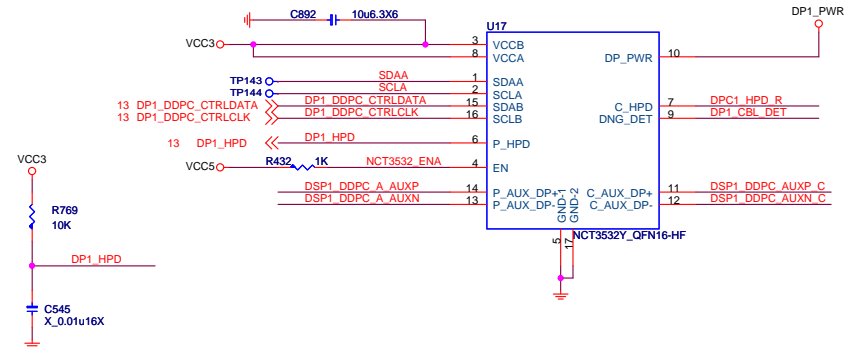


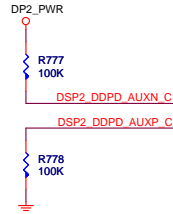
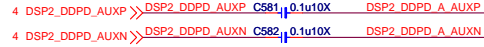
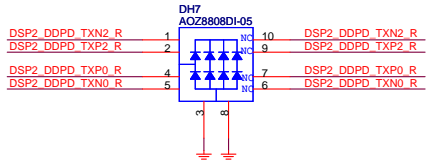
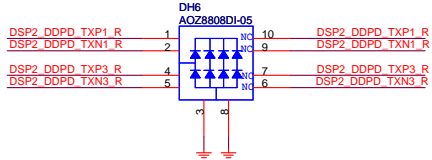
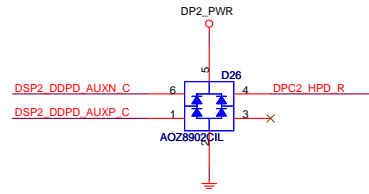


4 DSP1\_DDPC\_AUXP >> DSP1\_DDPC\_AUXP C567 0.1u10X DSP1\_DDPC\_A\_AUXP  
4 DSP1\_DDPC\_AUXN >> DSP1\_DDPC\_AUXN C566 0.1u10X DSP1\_DDPC\_A\_AUXN

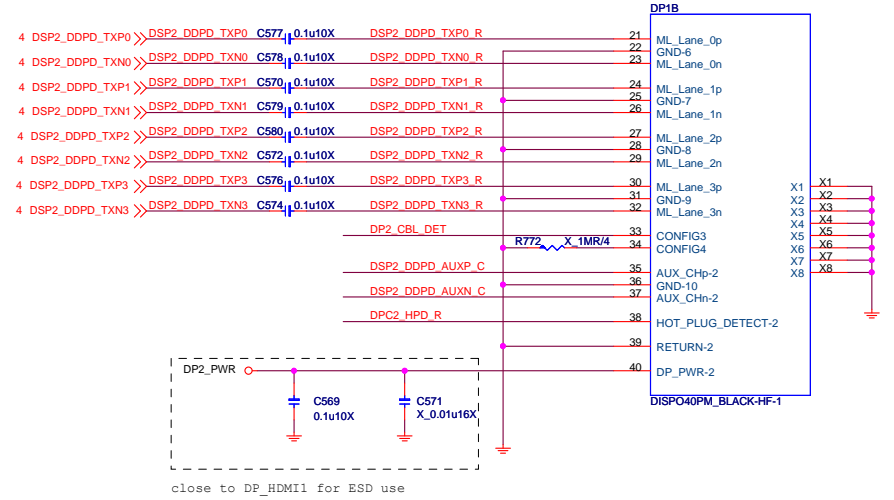


VCCB trace don't less than 30 mil

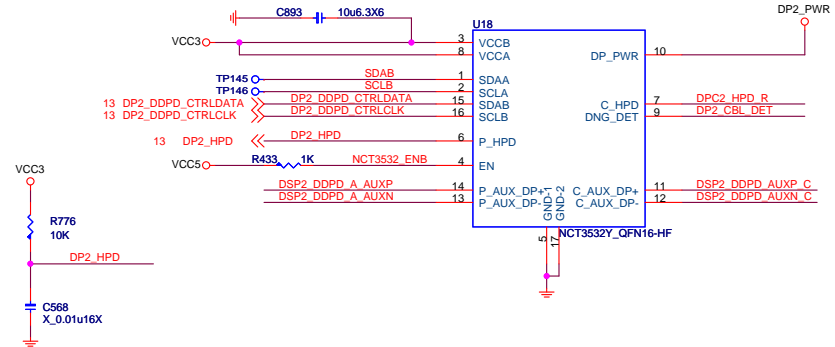




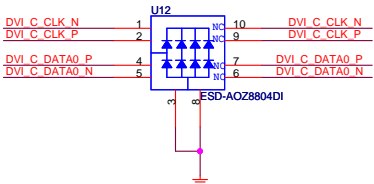
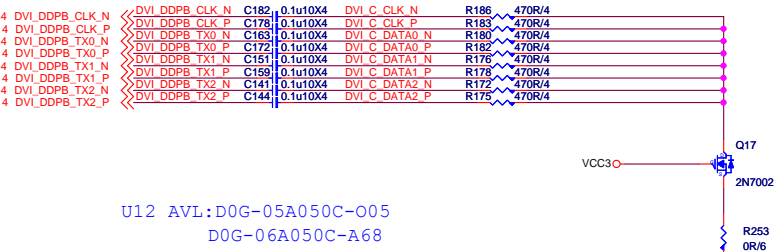
DP2 2015.10.20 Add



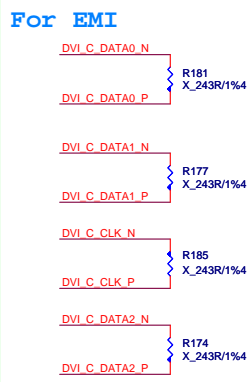
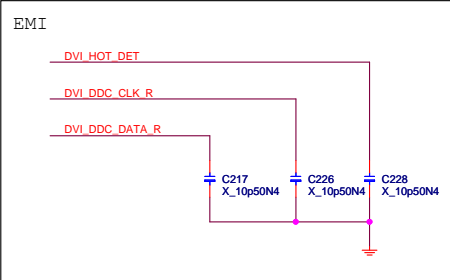
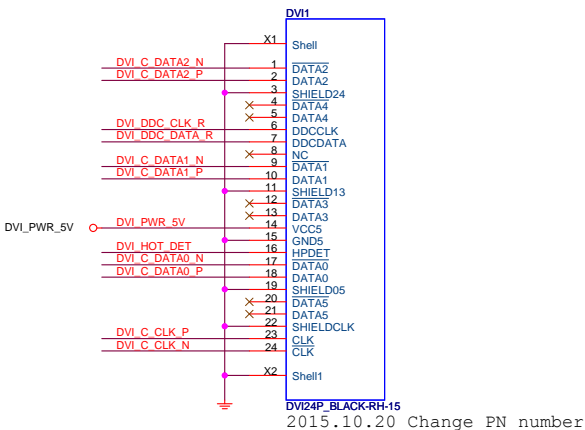
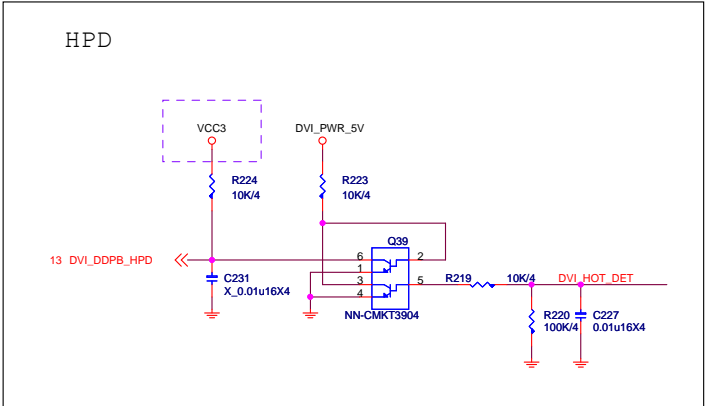
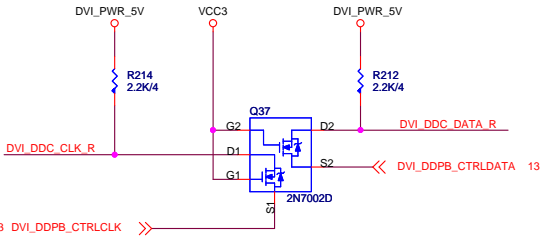
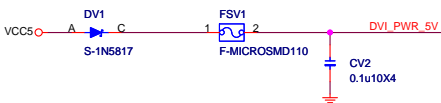
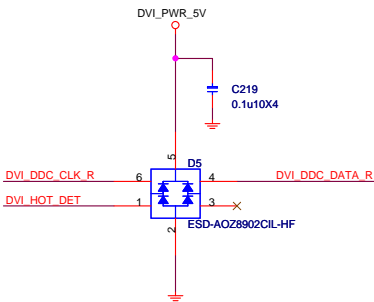
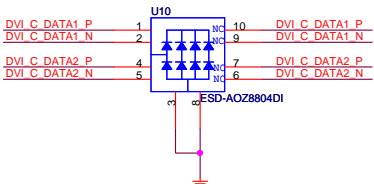
VCCB trace don't less than 30 mil

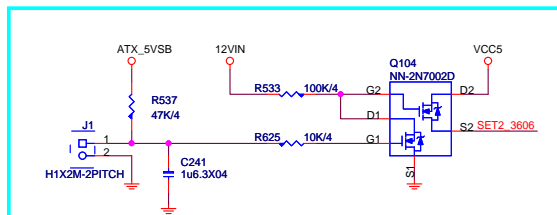
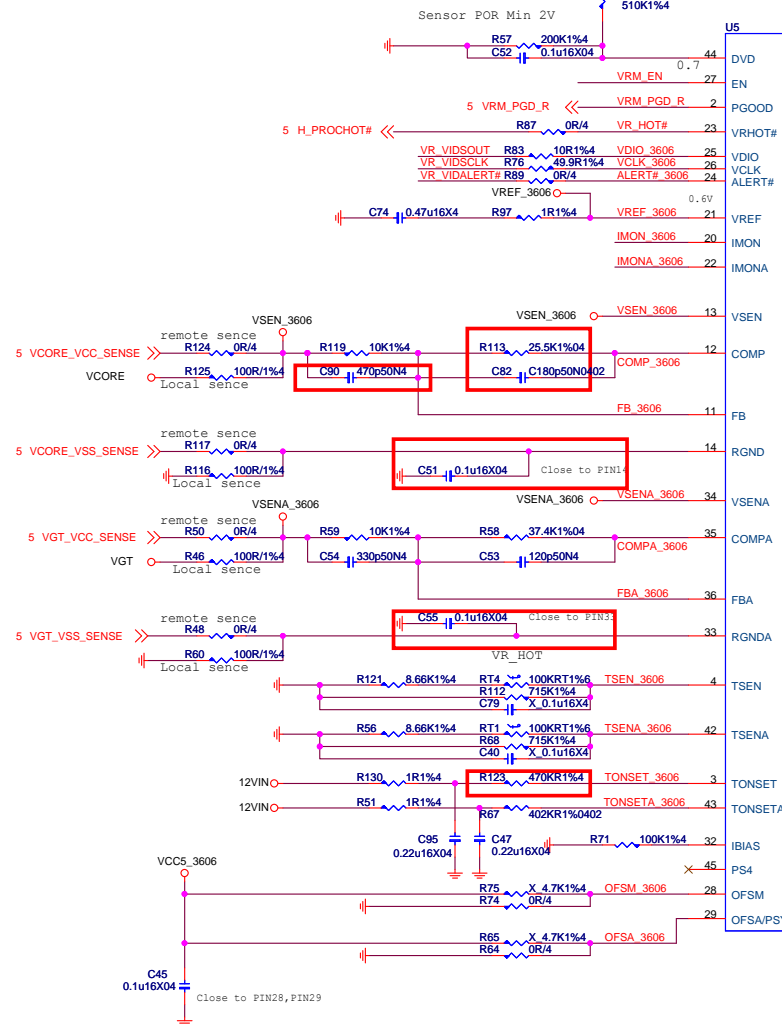
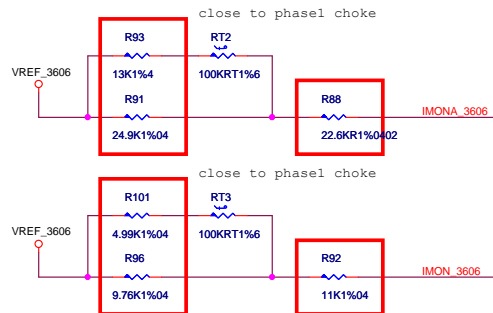
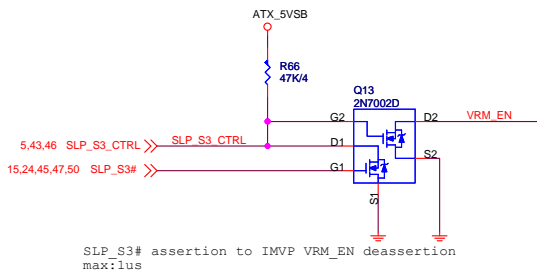
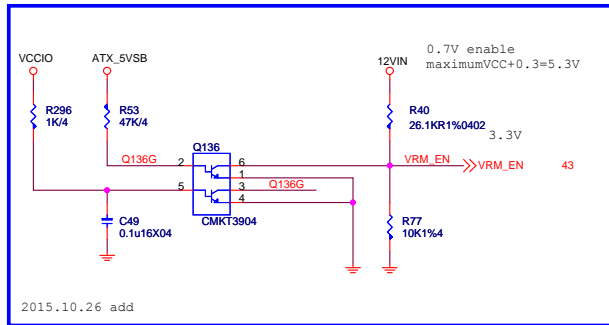
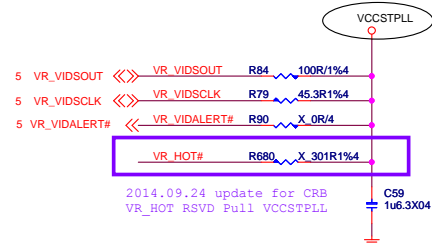


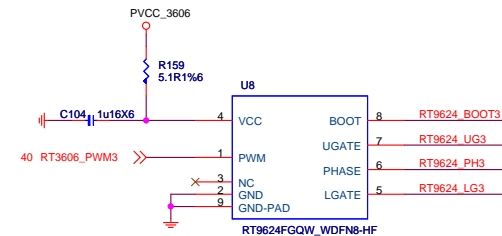
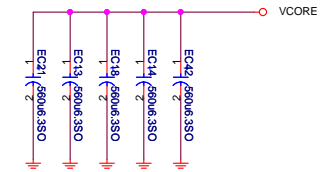
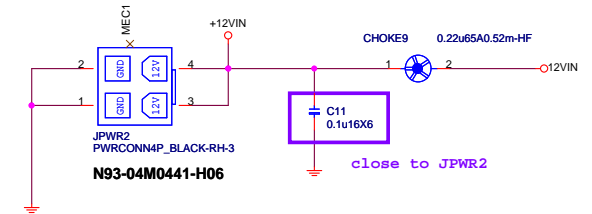
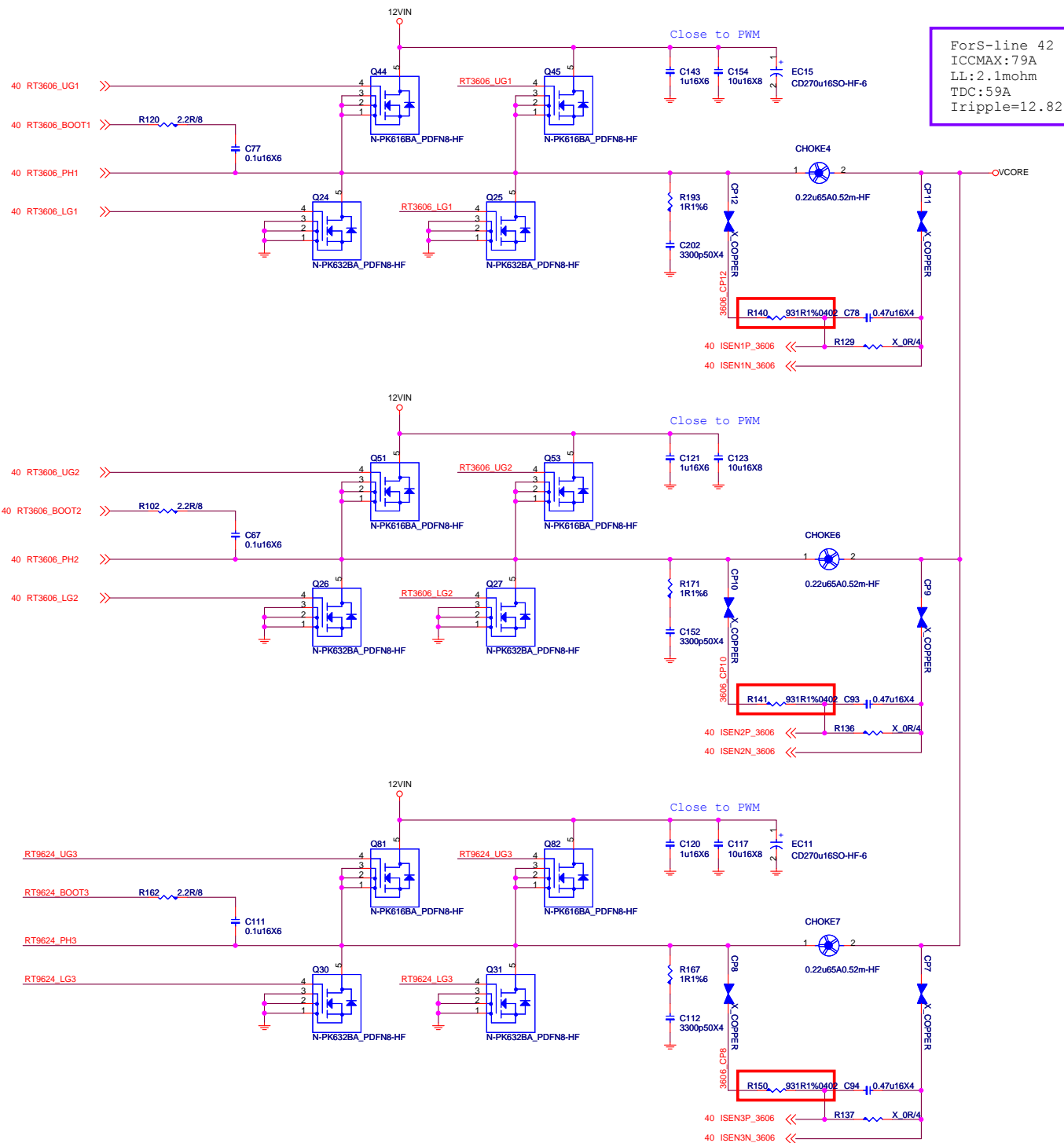
VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)



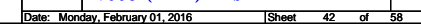
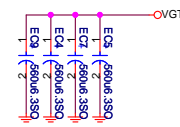
U10 AVL:D0G-05A050C-005  
D0G-06A050C-A68







TDC:56A



# SA Power:1.05V,12.3A

$$OCP = 12.3A * 1.4 = 17.22A$$

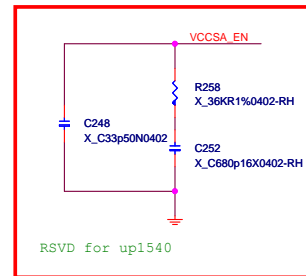
$$R_{ocs}(R15) = OCP * R_{dson}(Low\ side) 3.4m\Omega / 10\mu A$$

$$= 17.22 * (3.4m\Omega / 10\mu A)$$

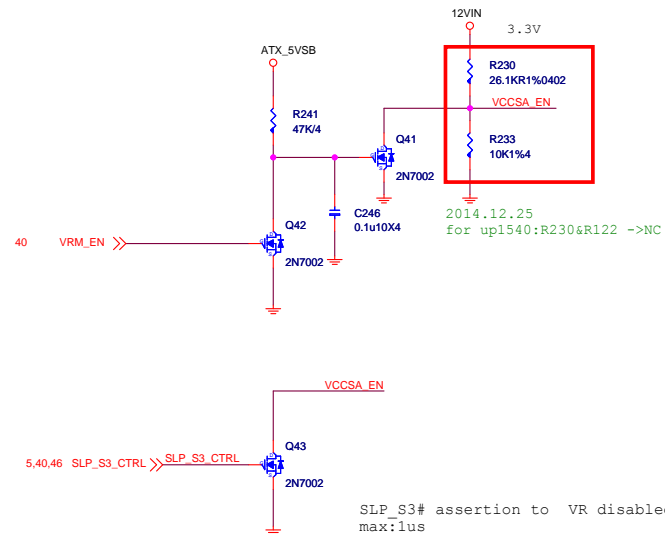
$$= 5.854K\Omega$$

Rocs:5.76K, OCP:  
D03-4C05N03-005 : 16.94A  
D03-632BA0C-N03 : 17.45A  
use UBIQ MOS need Check

Rdson(10V)  
D03-4C05N03-005 : 3.4mohm  
D03-632BA0C-N03 : 3.3mohm  
D03-3056M00-U47 : 4.2mohm



2015.01.22  
for up1540:stuff R258->36K,  
C248->33p, C252->680p  
for RT8125:R258.C248.C252->NC



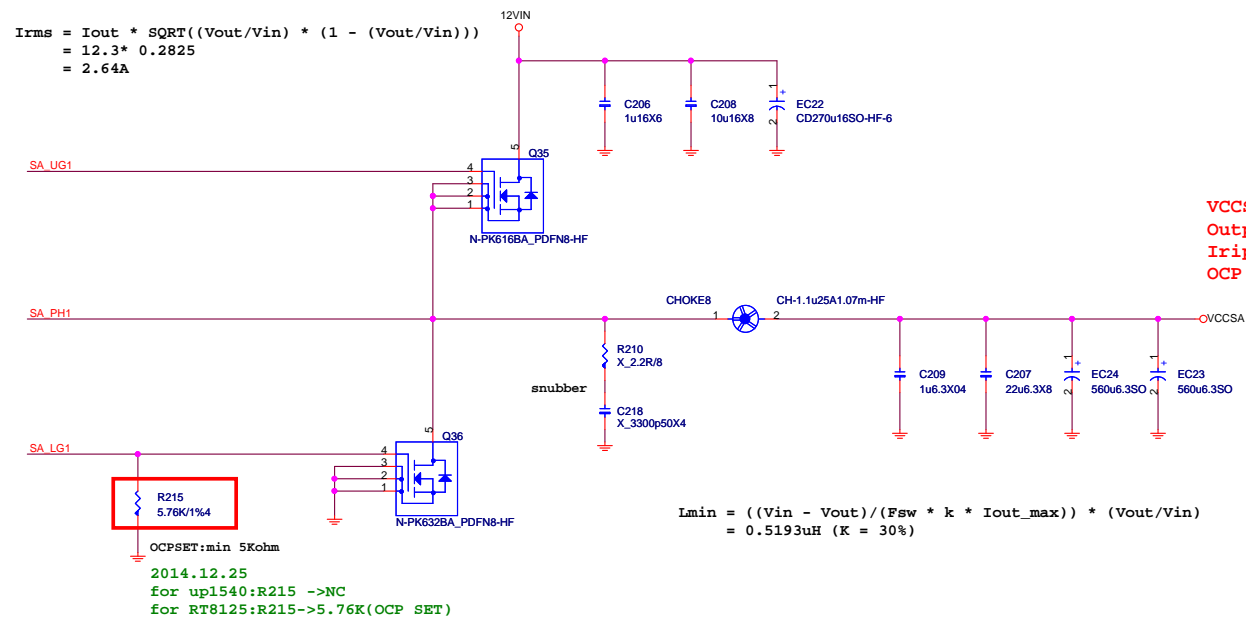
2014.12.25  
for up1540:C242&R234 ->NC  
for RT8125 C242:1000p, R234->1K

2014.12.25  
for up1540:R1039 is OCP set min:5K ohm  
stuff 5.36K OCP SET:15.76A  
for RT8125:R1039->1000p

$$I_{rms} = I_{out} * \sqrt{(V_{out}/V_{in}) * (1 - (V_{out}/V_{in}))}$$

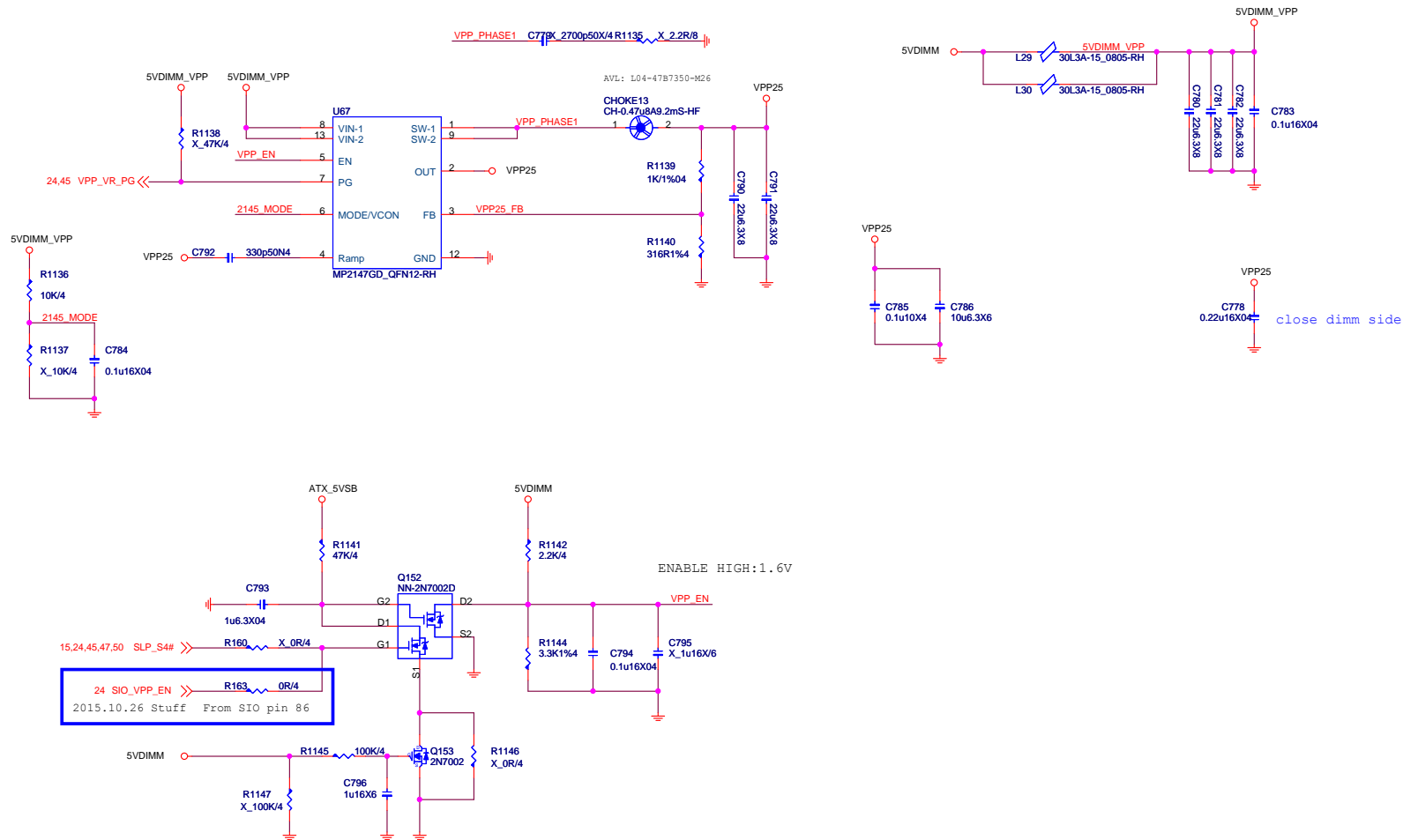
$$= 12.3 * 0.2825$$

$$= 2.64A$$



VCCSA:  
Output = 11.1A  
Irripple = A  
OCP = 15.54A

# 4DIMM :2.24A FOR DDR VPP2.5V







# VCCIO

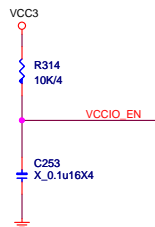
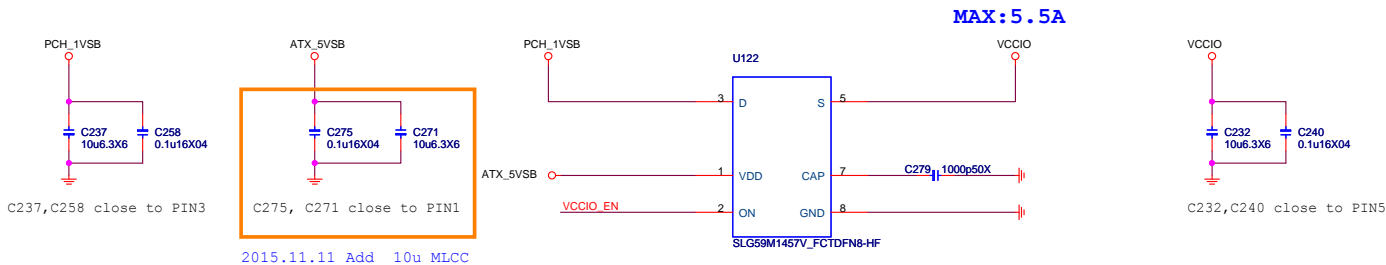
0.95V; 5.5A

IMAX 10A

ILIMIT=10A~12A

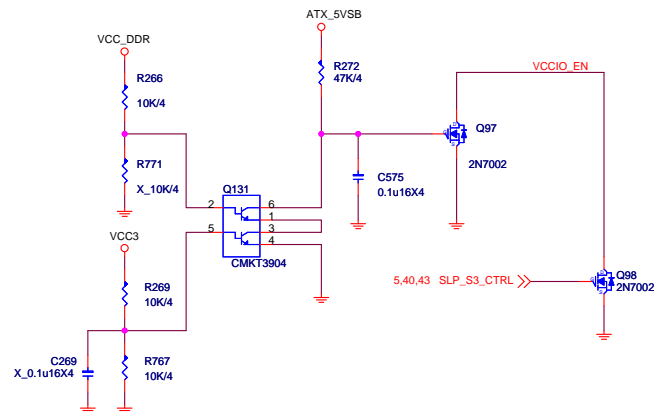
IOC=ILIMIT+40%\*IMAX/2=12A~14A.

0.7776uH<L<1.1664uH



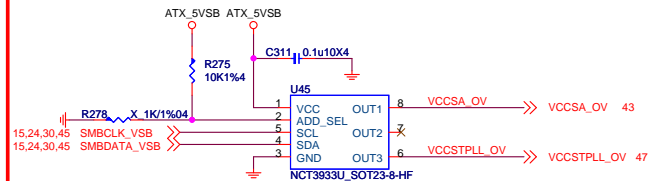
SLP\_S3# assertion to VCCIO VR disabled <1uS.

SLP\_S3# assertion to VCC, VCCGT, VCCIO and VCCSA rails completely off. <500ms



## UPI VOLTAGE CONSOLE

0x20:RL=OPEN,RH=10K



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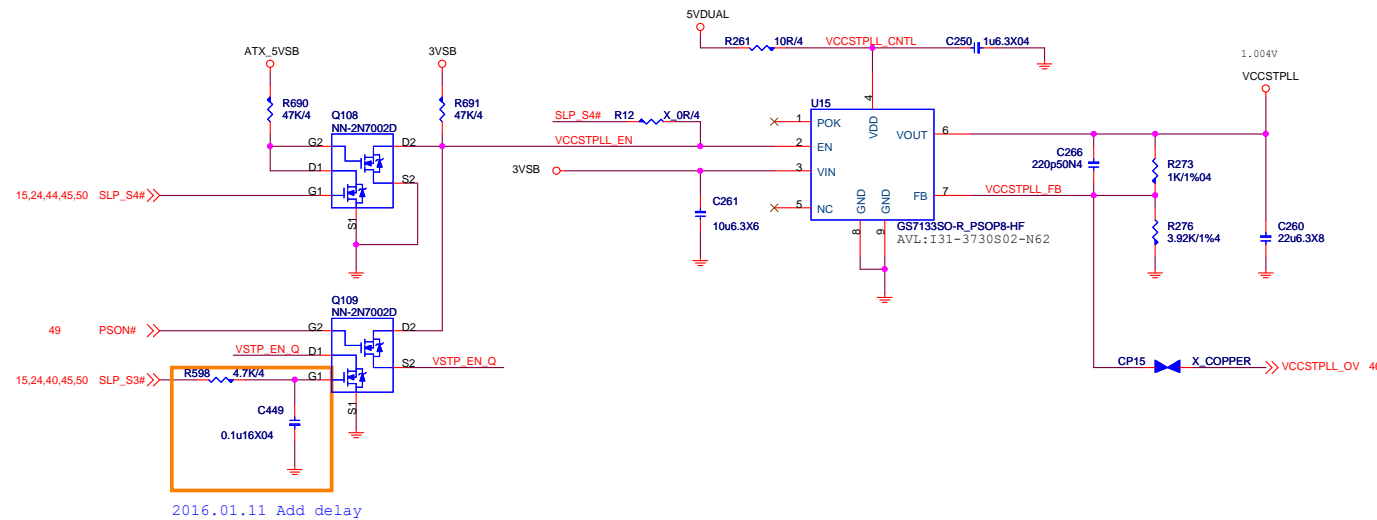
## VCCSTPLL

1.0V; 120mA

VCCIO ramped and stable before  
beginning of VCCOPC/VCCEOPIO ramp  
VCCST/PLL stable 1ms before PROCPWRGD  
For Cost down VCCST&VCCPLL merge

## VCCPLL\_OC

1.2V; 100mA



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# PCH\_1VSB

1.0V;

OCP = 21A

Rocset =  $1.5 * I_{max} * R_{dson(LOW)} / I_{ocset}$   
 =  $1.5 * 14.75 * 5mohm / 10uA$   
 = 7.998K

Rocs:5.9K,OCP:

D03-4C05N03-005 : 11.8A

D03-632BA0C-N03 : 12.82A

use UBIQ MOS need Check

Rdson(LOW)4.5V

D03-4C05N03-005 : 5 mohm

D03-632BA0C-N03 : 4.6mohm

D03-3056M00-U47 : 6.2mohm

2015.01.22  
 for up1540:R323->2.2R  
 for RT8125:R323->10R

$$I_{rms} = I_{out} * \sqrt{(V_{out}/V_{in}) * (1 - (V_{out}/V_{in}))}$$

$$= 10.664 * 0.4$$

$$= 4.2656A < 5000mA$$

MAX:9.25A +5.5A

$$I_{min} = ((V_{in} - V_{out}) / (F_{sw} * k * I_{out\_max})) * (V_{out}/V_{in})$$

$$= 0.8335uH (K = 30\%)$$

$$V_{out} = V_{ref} * (1 + R_{107}/R_{112})$$

$$= 0.8 * (1 + 1K/3.92K)$$

$$= 0.8 * 1.2551$$

$$= 1.004V$$

0728: add

2014.12.25  
 for up1540:R329 ->NC

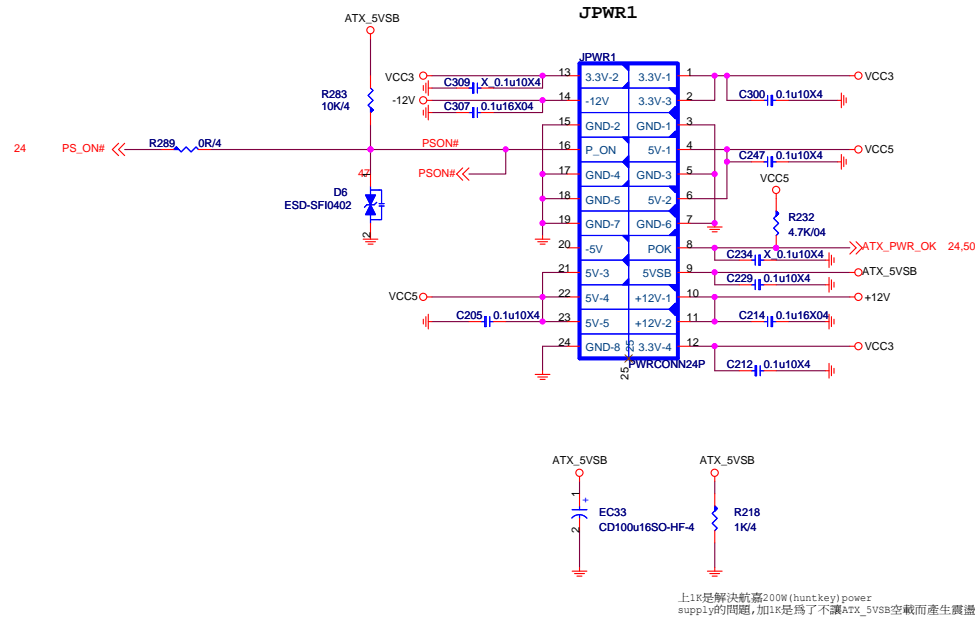
0728: Change net name

2015.01.22  
 for up1540:stuff R327->36K,  
 C353->33p,C356->680p  
 for RT8125:R327.C353.C356->NC

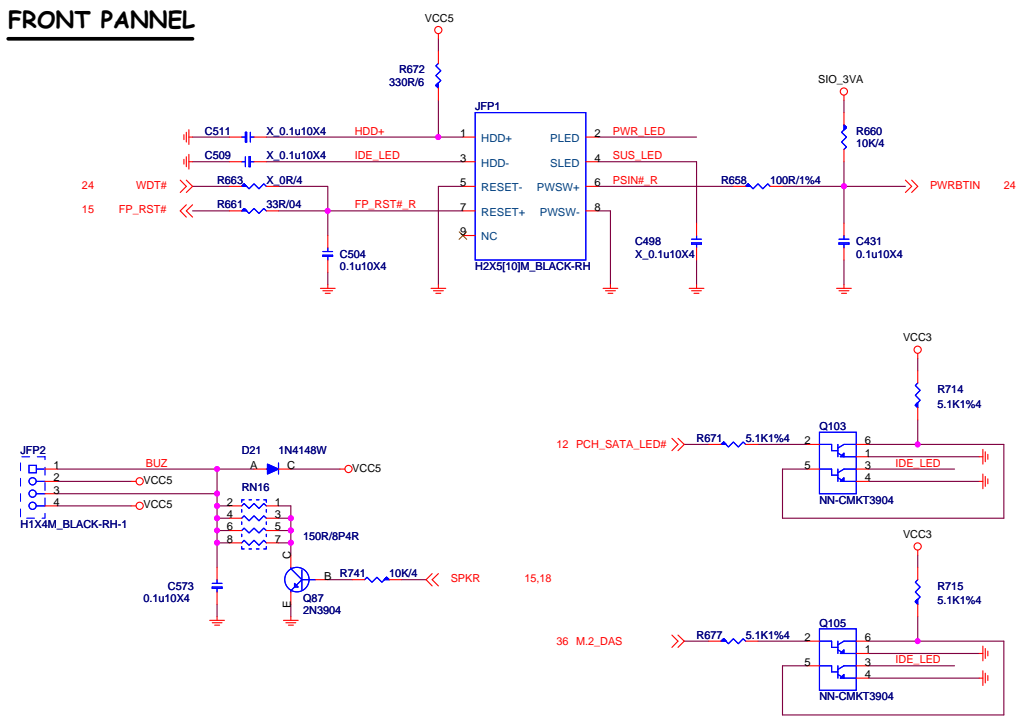
0902 : Stuff R when NO PCH\_1P8 & V\_OPC\_1P8

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Size Custom	Document Description PCH Core power_uP1540	Rev 0A
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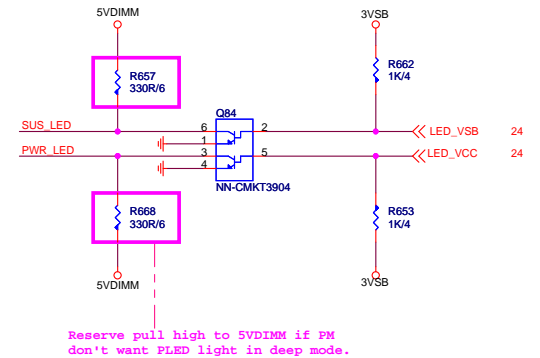
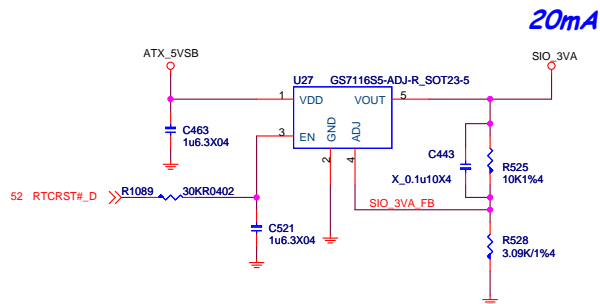
## ATX POWER CONNECTOR



## FRONT PANNEL



## MSI\_LED

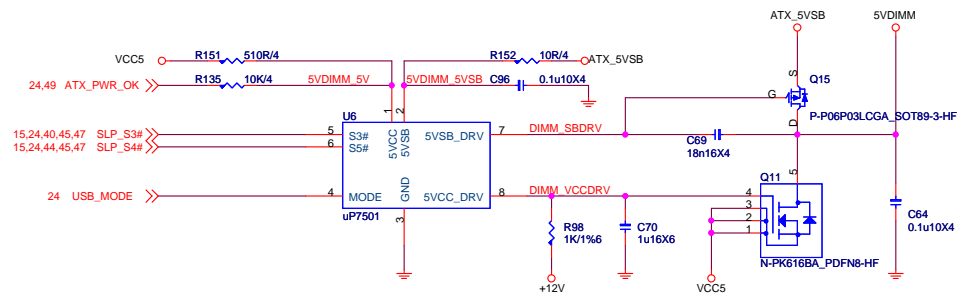


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## 5VDIMM FOR DDR

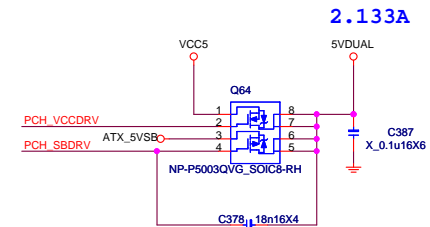
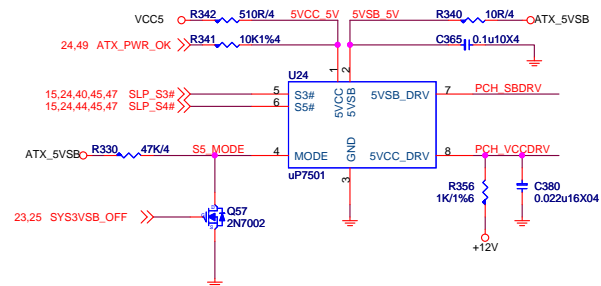


7501 Mode  
H:Support S0/S3/S5  
L:Support S0/S3

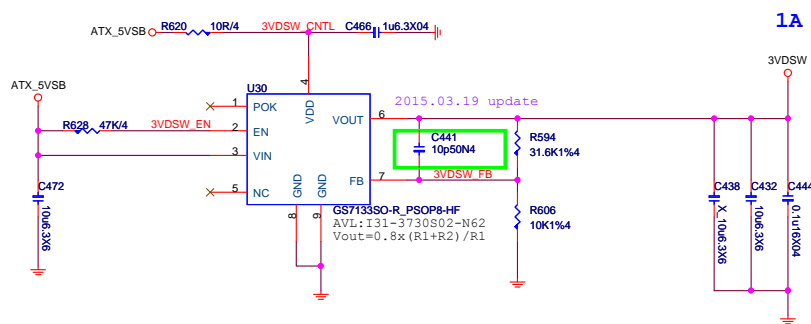
DIMM\_VCCDRV >> DIMM\_VCCDRV 32  
DIMM\_SBDV >> DIMM\_SBDV 32

## 5VDUAL

5VDUAL is power source of LP0SB

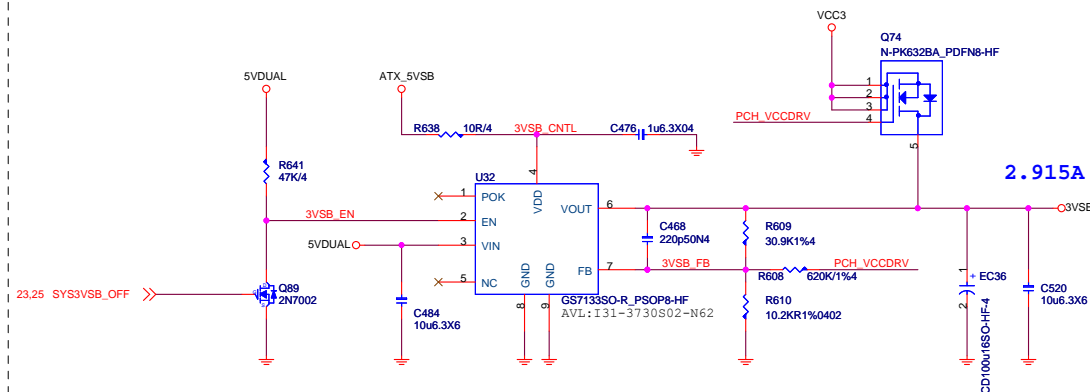


## 3VDSW



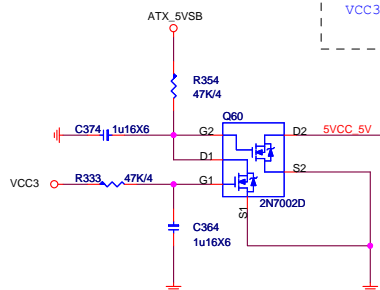
1A

## 3VSB cost down

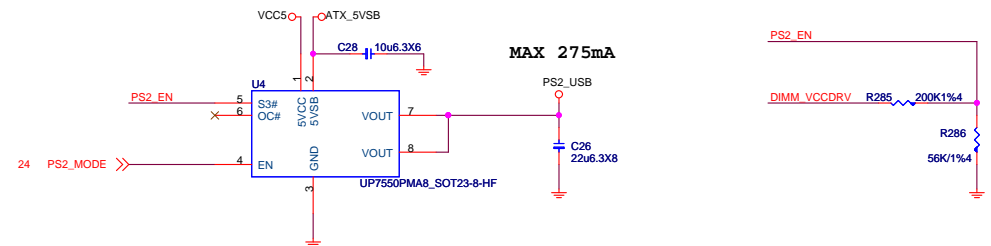


VFB=3.224V for S0->S3 3VSB voltage raise & ATX\_5VSB drop.

For power 700W solution (only for uP7501+uP7506 for 3VSB solution)  
The power supply VCC3 delay 12ms after VCC5 assert.  
The chip U7501 5VDRV1 work when the VCC5 ready  
(When VCC5 up to 4.2V and the 5VDRV1 delay 6ms assert), but  
VCC3 not ready and let the 3VSB sequence fail.



## PS2 Power

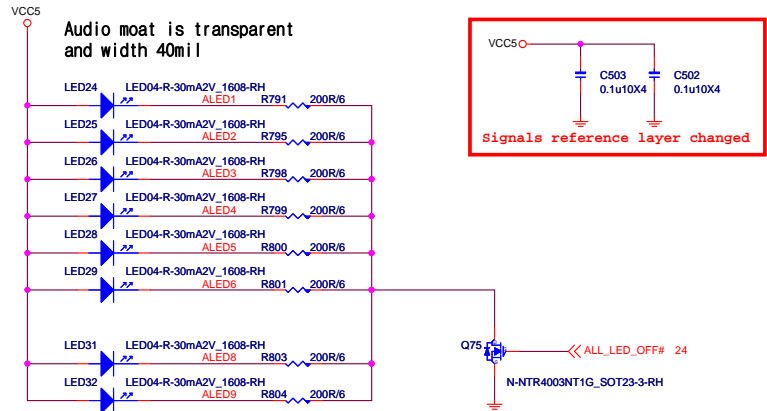


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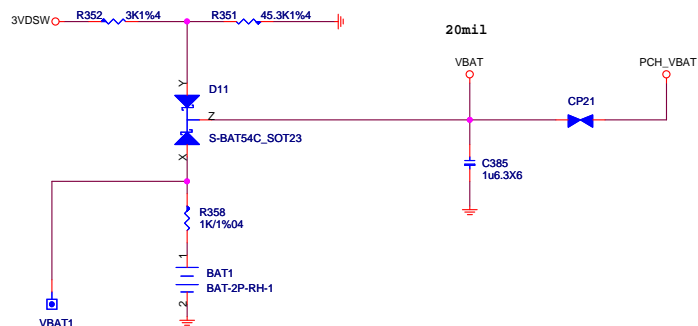
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2015.10.22 Remove Side LED

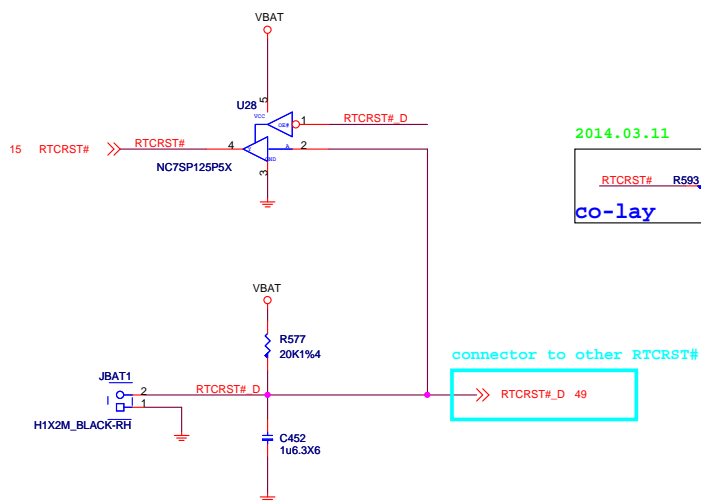
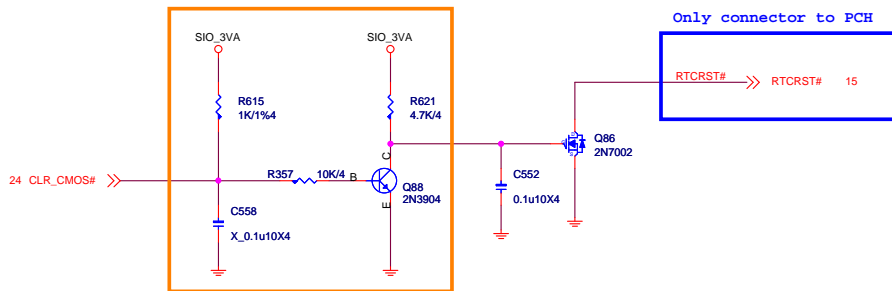


此測點請放背面



## BIOS MODE

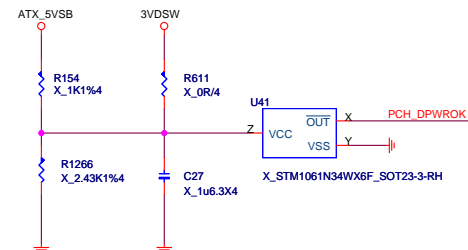
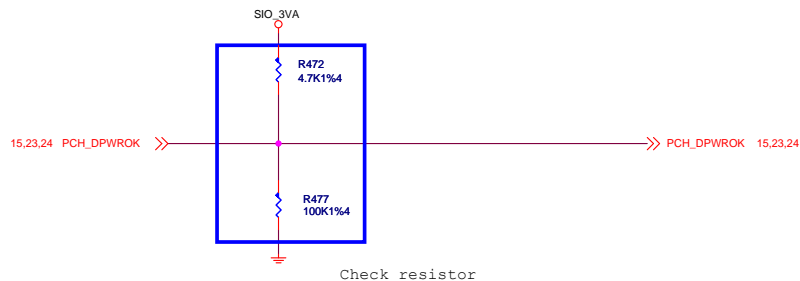
2015.4.24 updata CLR\_COMS circuit



2014.03.11

co-lay

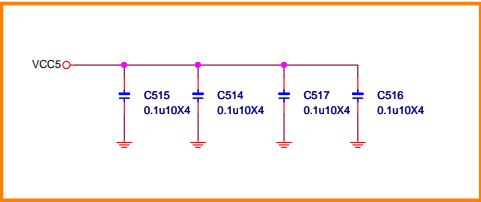
tri-state		
INPUT		outout
PIN1	PIN2	pin4
L	H	H
L	L	L
H	X	Z

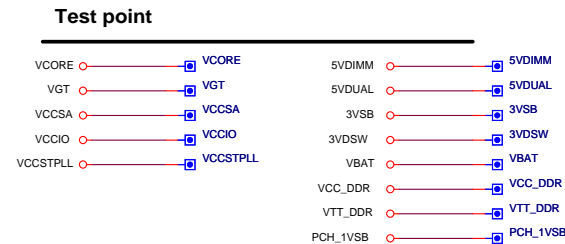
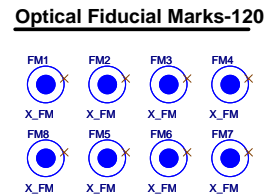
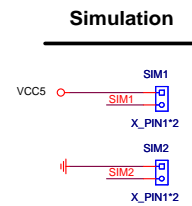
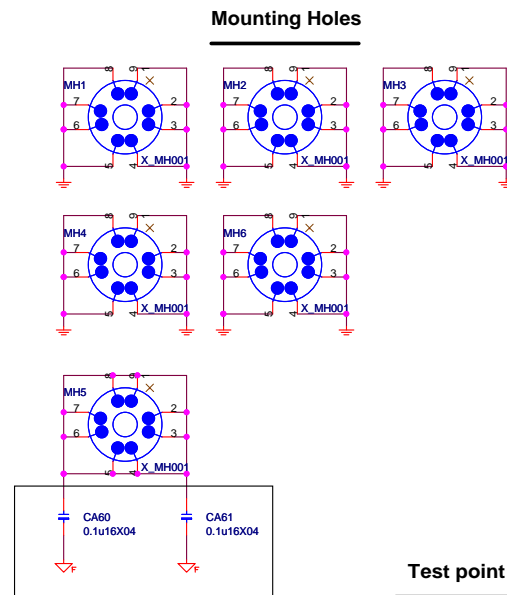
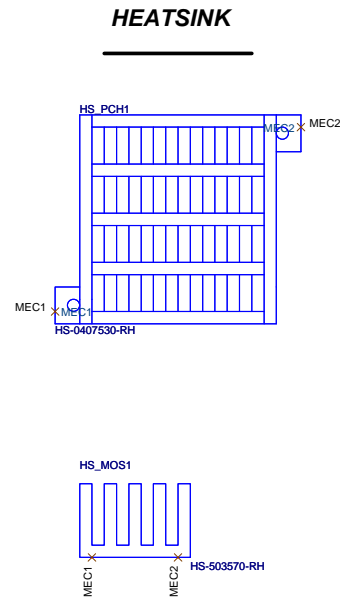
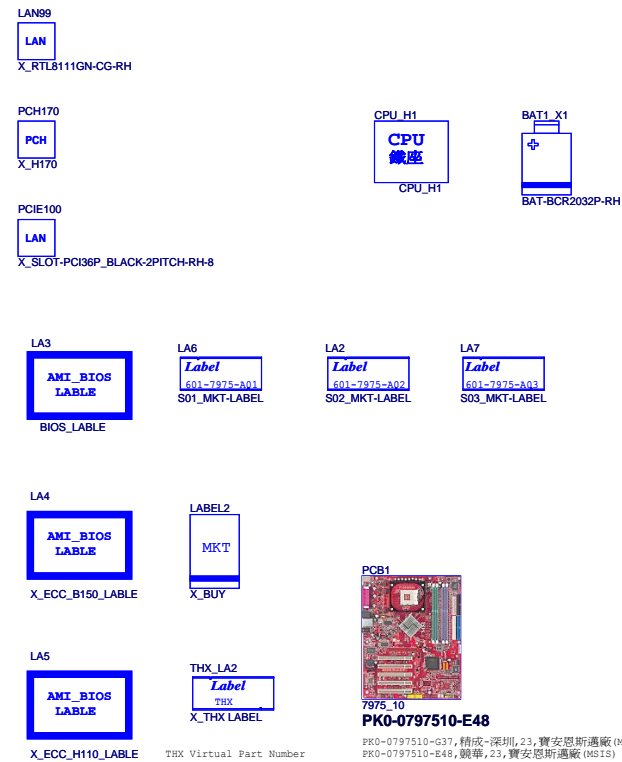


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SIO 5V plane EMI CAP





MS-7975-0A 主BOM為B150

OPT	Configure	BOM	Function
STD	B150	601-7975-A01	MS-7975 0A,B150,LGA1151, 2DDR3,2DDR4,1PCI-Ex16,2PCI-Ex1,4SATA3,6USB3, HD Audio,Gb LAN,DSUB,DVI,HDMI
SKUA	B150	601-7975-A02	
SKUB	H170		



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